

COMPAL CONFIDENTIAL

MODEL NAME :CDM60

PCB NO : LA-E071P

BOM P/N :

BR12 KBL-U UMA

Kabylake U

2016-11-07

REV : 1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

www.teknipedia.com

MB PCB

Part Number	Description
DAA000C0000	PCB 1SR LA-E071P REV0 MB 1

Layout Dell logo



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REV:X00
PWB: 9RJMF

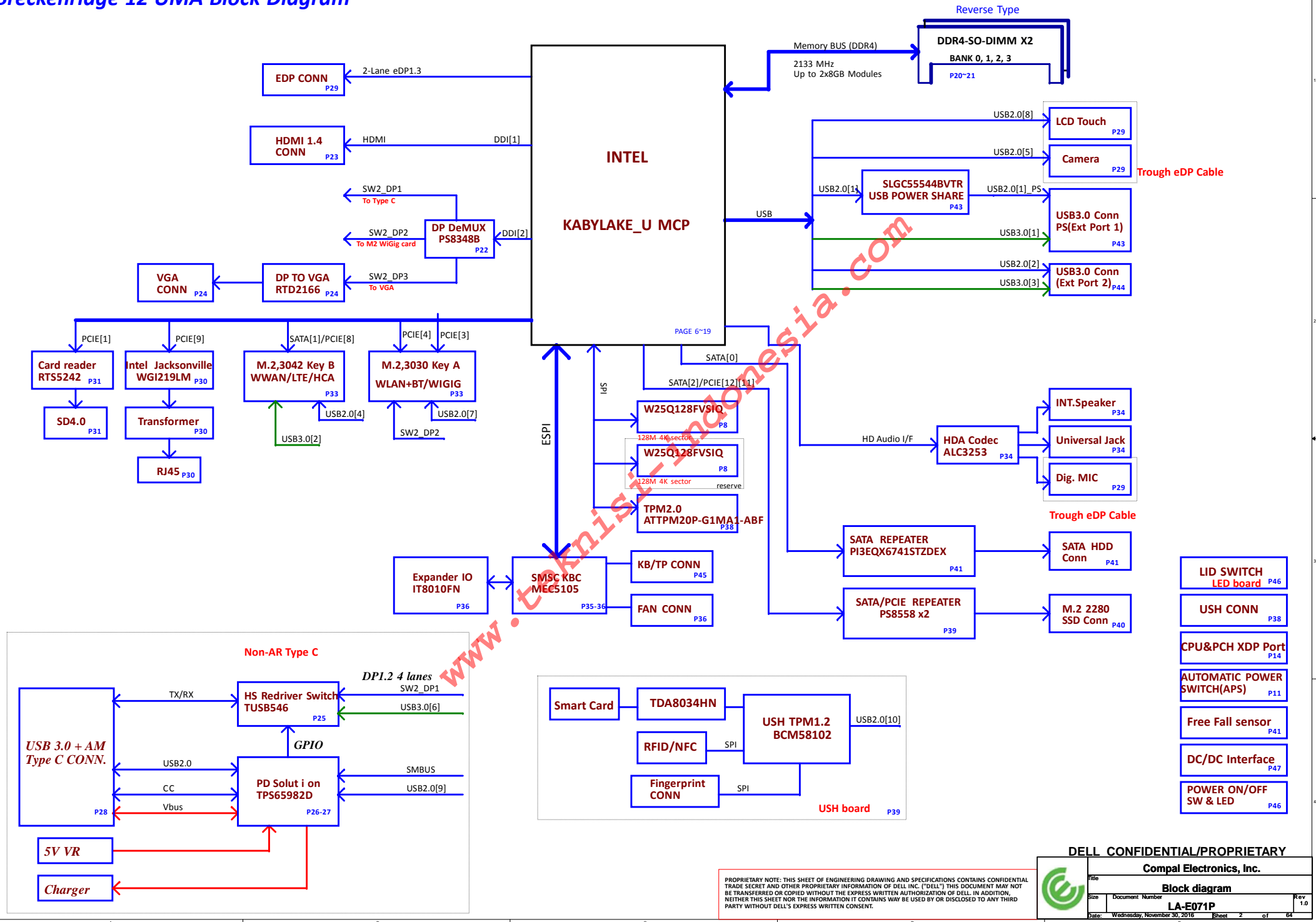
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Breckenridge 12 UMA Block Diagram



POWER STATES

Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
State									
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State	power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON	ON
S3	ON	ON	OFF	OFF
S5 S4/AC	ON	OFF	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.5
			Add Plating		
1	Top		Copper foil	0.5oz+plating	1.6
		3.8	Prepreg	1080	2.6
2	GND		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
3	IN 1		Copper foil	1oz	1.25
		3.7	Prepreg	2116H	4.3
4	GND/PWR		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
5	IN 2		Copper foil	1oz	1.25
		3.6	Prepreg	1080H x2 orPP2116HRC	4.2
6	IN 3		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
7	GND/PWR		Copper foil	1oz	1.25
		3.8	Prepreg	2116H	4.3
8	IN 4		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
9	GND		Copper foil	1oz	1.25
		3.8	Prepreg	1080	2.6
10	Bottom		Copper foil	0.5oz+plating	1.6
			Add Plating		
			SolderMask	IT-158	0.5
Overall Thickness (1.2mm ± 10%)					47.68000
					1.211072

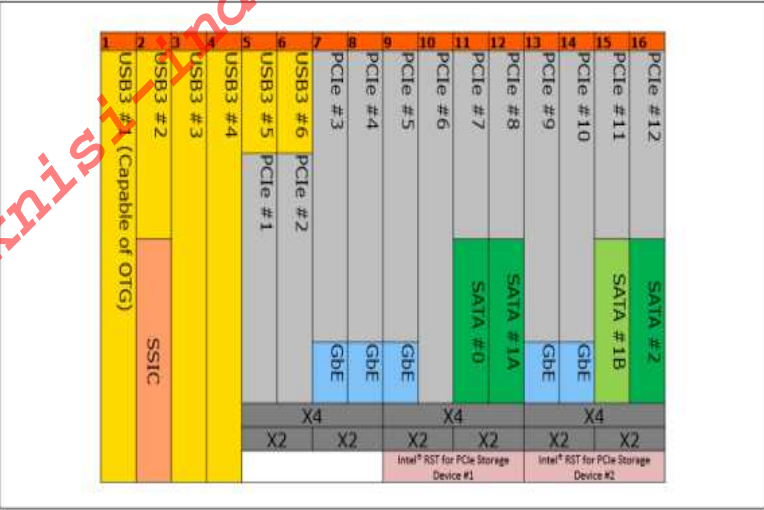
For Breckenridge12/14/15 UMA

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Lef t
USB3.0-4				JUSB3-->Rear Lef t
USB3.0-5		PCIE-1		Card Reader
USB3.0-6		PCIE-2		Type-C Port
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		M.2 3030(WIGIG)
		PCIE-5		NA
		PCIE-6		NA
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	M.2 3042(SATA Cache or HCA)
		PCIE-9		LOM
		PCIE-10		NA
		PCIE-11	SATA-1*	M.2 2280 SSD (PCIex2 or SATA)
		PCIE-12	SATA-2	

12" not support JUSB3

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2-->Lef t
3	JUSB3-->Rear Lef t
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	Type-C Port
10	USH

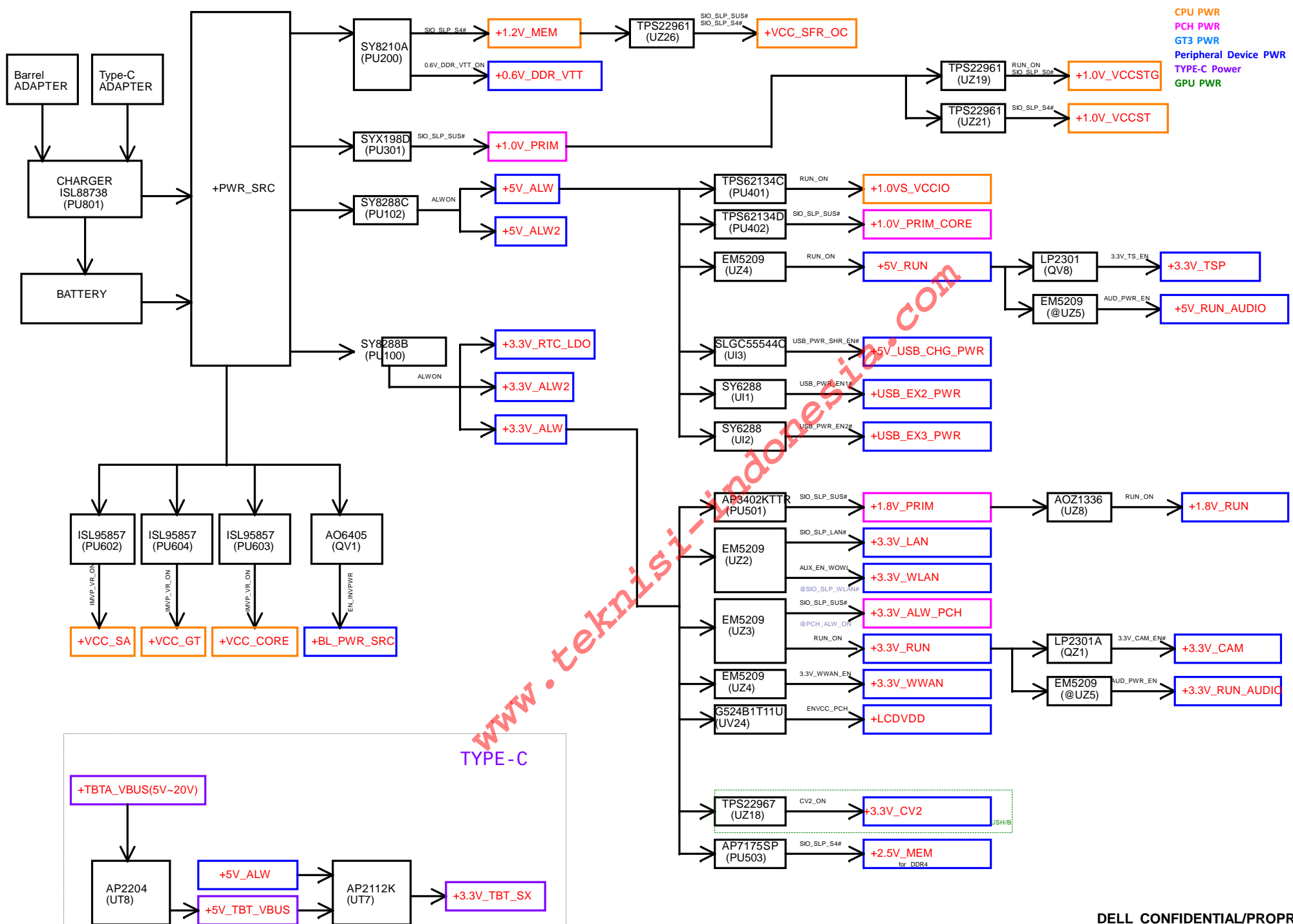
High Speed I/O (HSIO) Lane Multiplexing in KBL U



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Port assignment	
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CPU PWR
PCH PWR
GT3 PWR
Peripheral Device PWR
TYPE-C Power
GPU PWR

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Power rails

LA-E071P

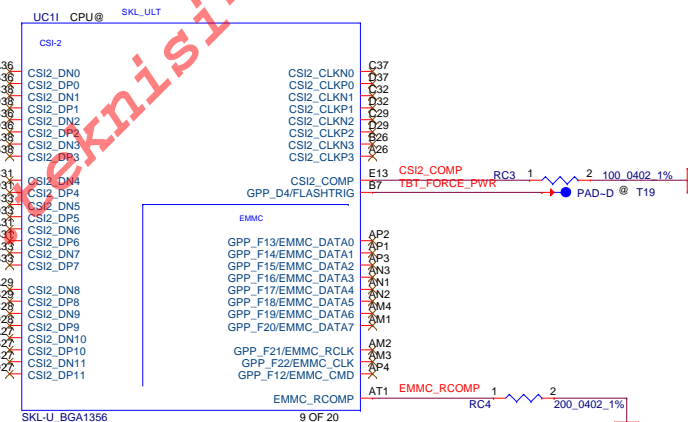
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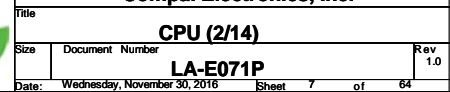
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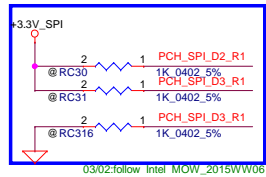
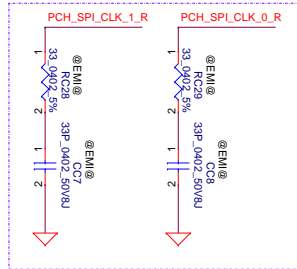
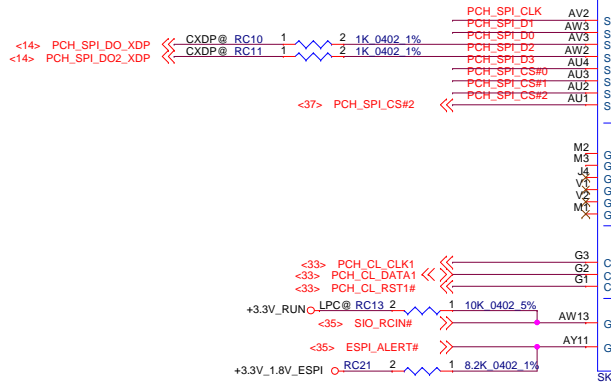


EDP
Timing=25mil,
SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0

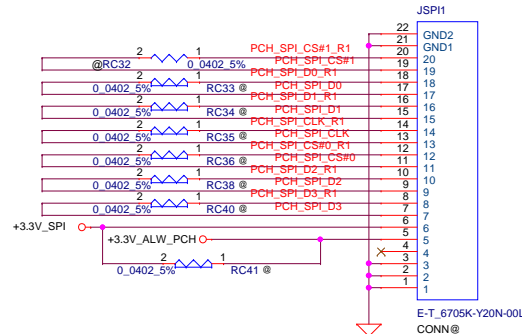
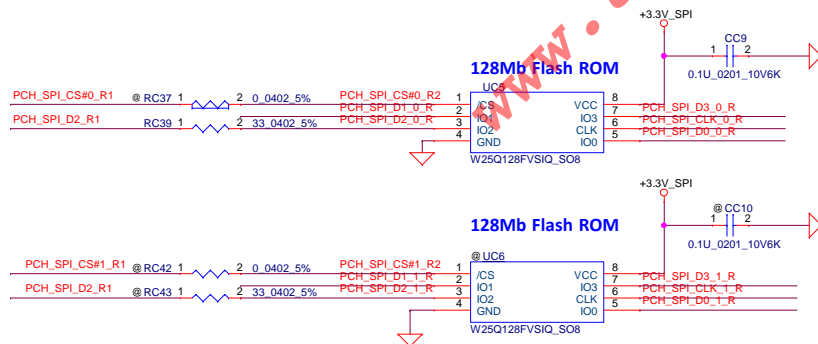
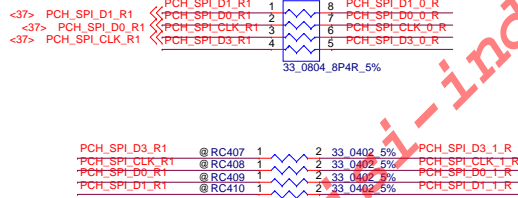
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K#1	→	DDR_B_CLK#1	<21>
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K#1	→	DDR_B_CLK1	<21>
KE0	→	DDR_B_CKE0	<21>
KE1	→	DDR_B_CKE1	<21>
KE2	→	PAD-D @ T5	
KE3	→	PAD-D @ T6	
CS#0	→	DDR_B_CS#0	<21>
D#1	→	DDR_B_CS#1	<21>
DT0	→	DDR_B_ODT0	<21>
DT1	→	DDR_B_ODT1	<21>
A5			
A9			
A6			
A8			
A7			
B0	→	DDR_B_BG0	<21>
A12	→		
T#E	→	DDR_B_ACT#	<21>
B1	→	DDR_B_BG1	<21>
A13			
A15			
A14			
A16			
B0	→	DDR_B_BA0	<21>
A2	→		
A10	→	DDR_B_BA1	<21>
A1			
A0			
A3			
A4			
QS#2			
QS2			
QS#3			
QS3			
QS#6			
QS6			
QS#7			
QS7			
QS#2			
QS2			
QS#3			
QS3			
QS#6			
QS6			
QS#7			
QS7			
ERST#			
DR21_PAR,DDR1_ALERT# for DDR4			
DRRTY	→	DDR_B_ALERT#	<21>
DRMST#	→	DDR_B_PARITY	<21>
P1	→	DDR_DRAMRST#	<20>
P2			



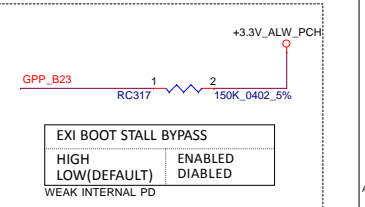
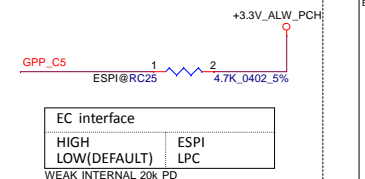
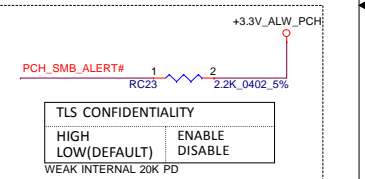
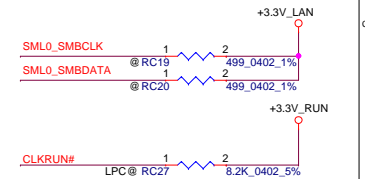
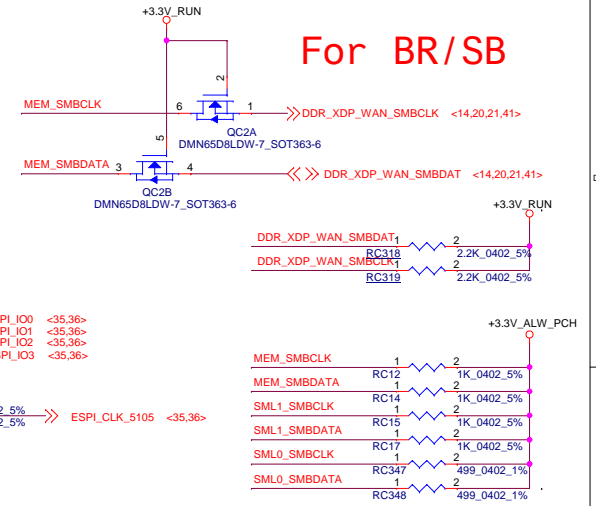
SPI_MOSI= SPI_I00
SPI_MISO= SPI_I01
PCH_EDS R0.7 p.235~236



SOFTWARE TAA



For BR/SB



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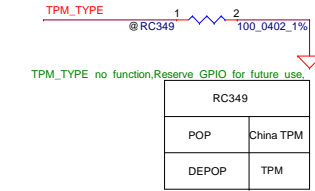
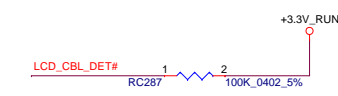
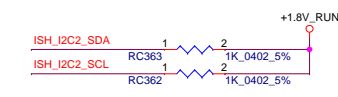
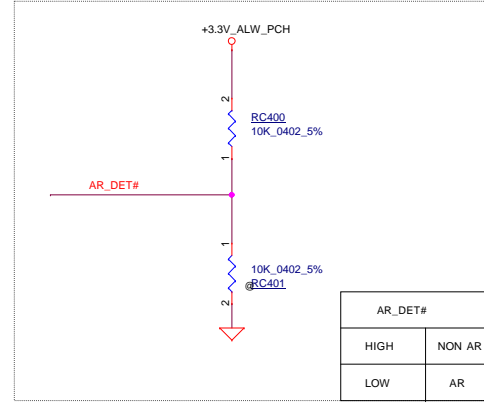
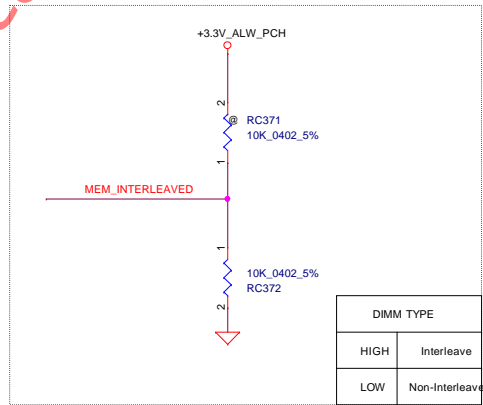
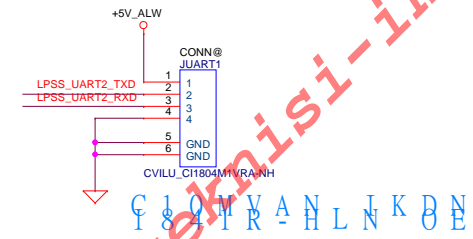
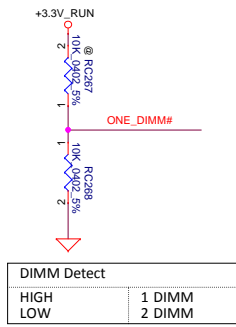
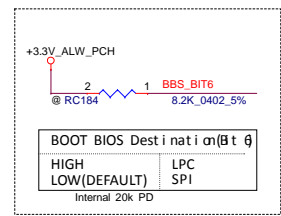
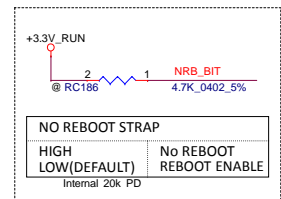
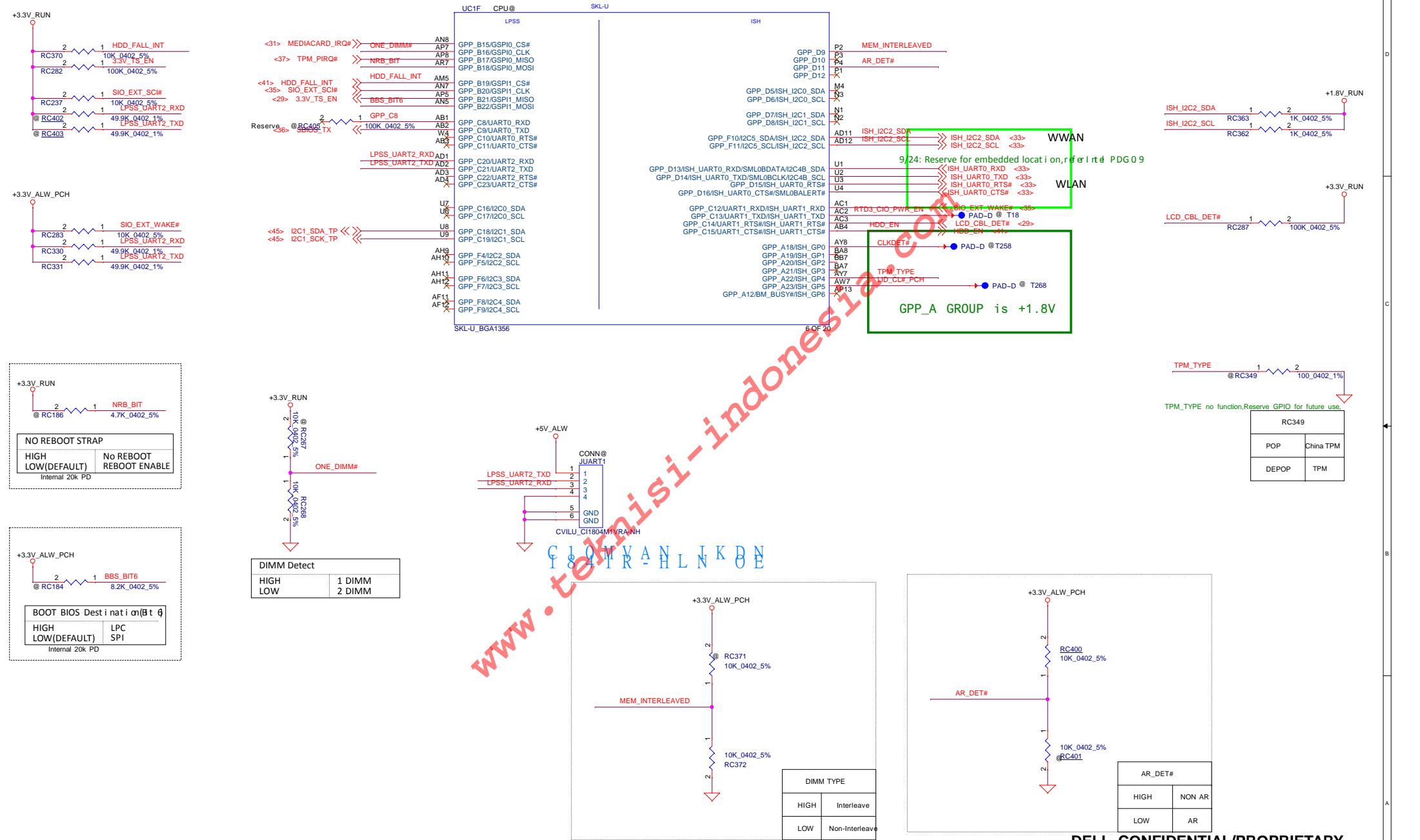
CPU (3/14)

LA-E071P

Rev 1.0

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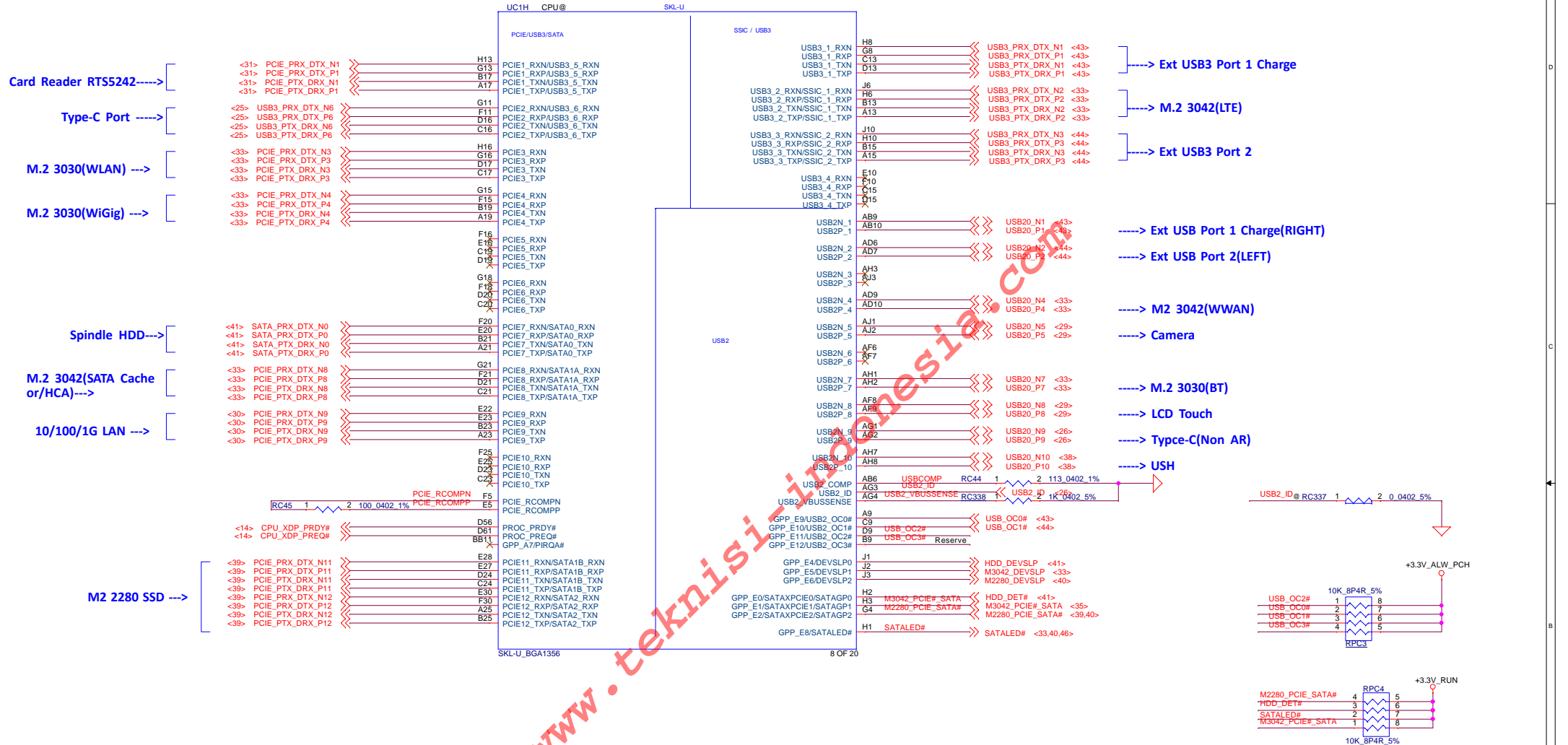
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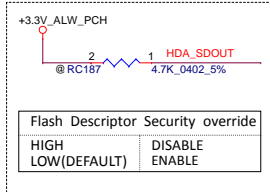
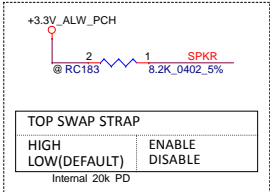
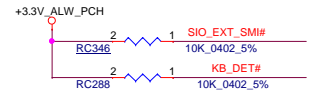
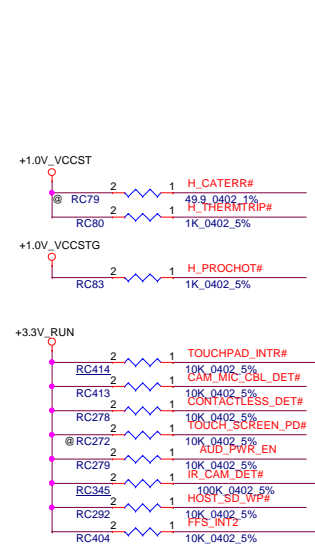
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For NON AR, Breckenridge 12/14/15 UMA

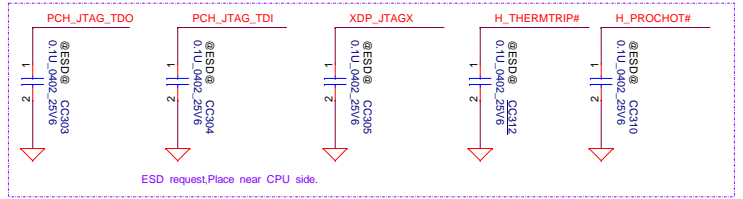
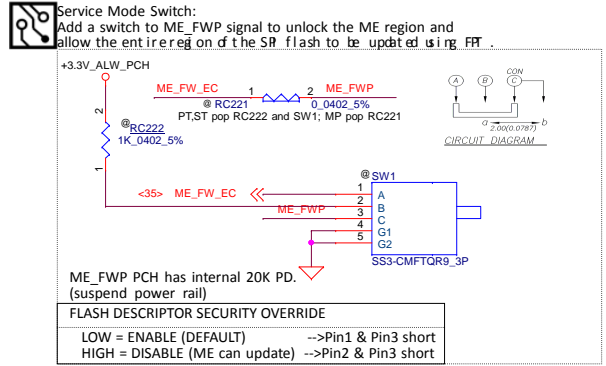
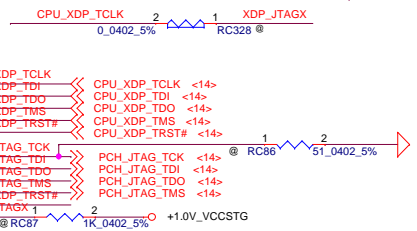
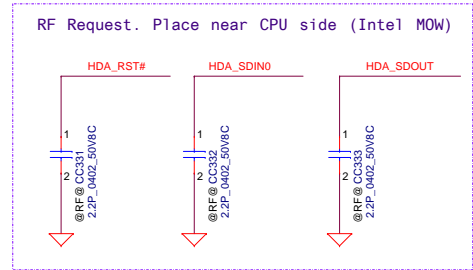
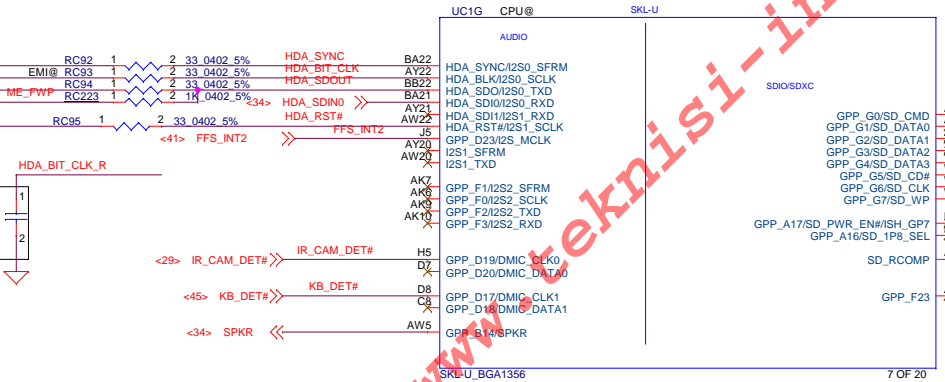




TOP SWAP STRAP	
HIGH LOW(DEFAULT)	ENABLE DISABLE
Internal 20k PD	

Flash Descriptor Security override	
HIGH LOW(DEFAULT)	DISABLE ENABLE

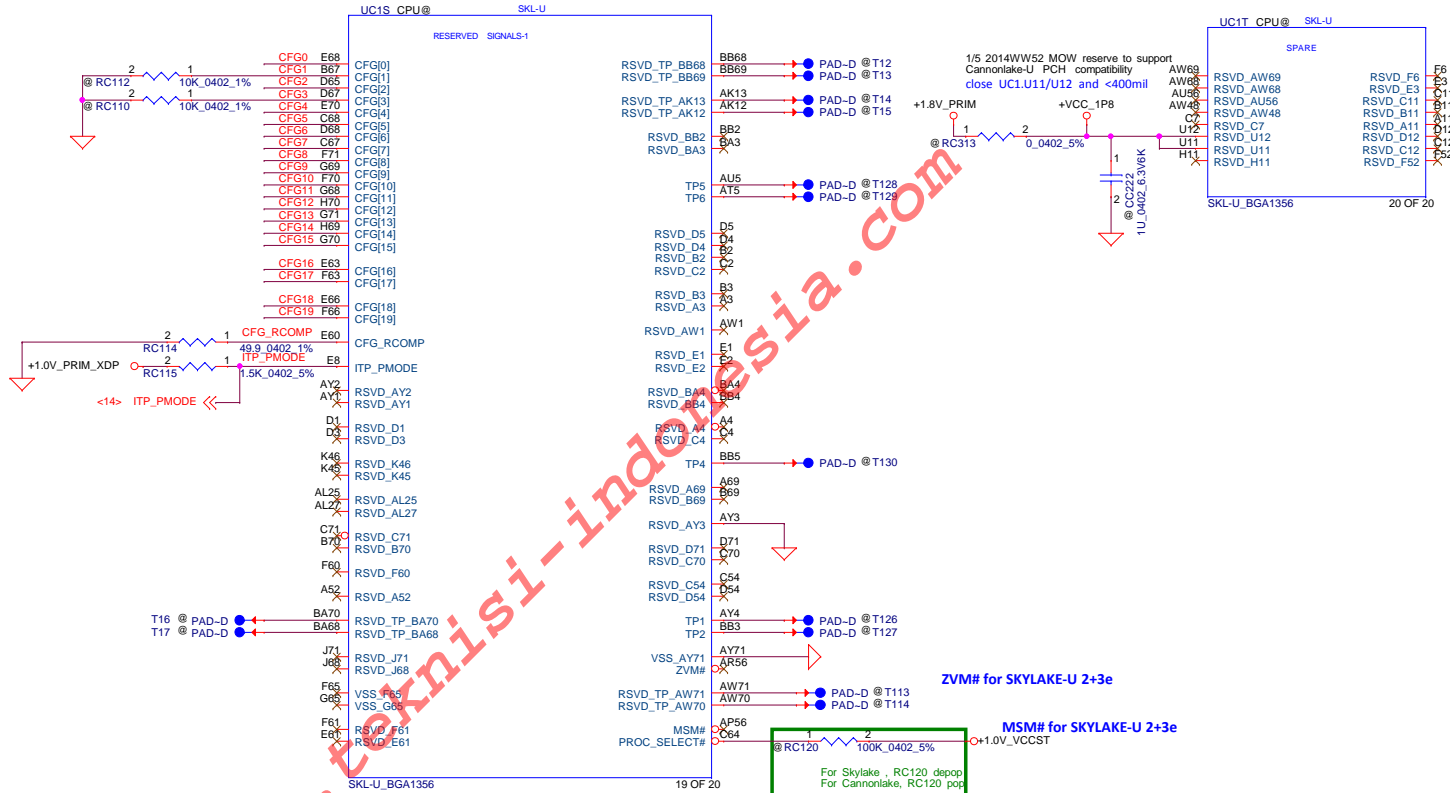
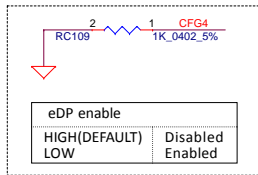
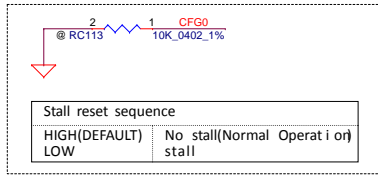
TOUCH_SCREEN_PD# don't move to RPC,



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<14> CFG0[0..19]

CFG2[5][6][7] for SKYLAKE-H CPU CFG strap pin



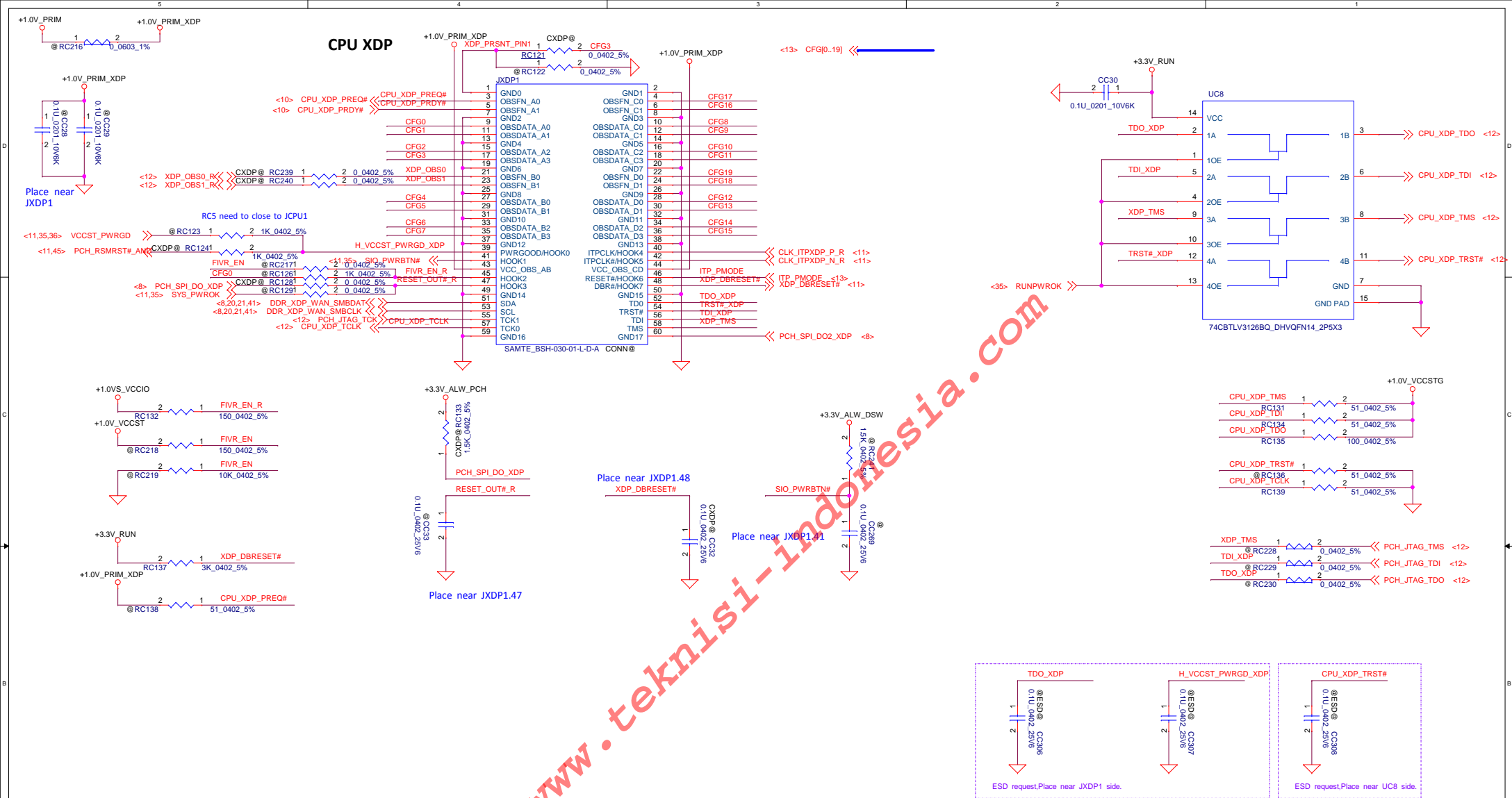
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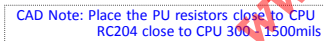
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+VCC_CORE +VCC_CORE



Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source



**CAD Note: Place the PU resistors close to CPU
RC208close to CPU 300 - 1500mils**

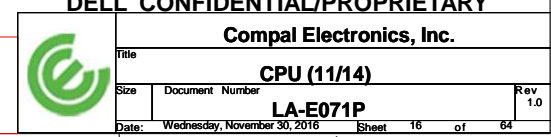
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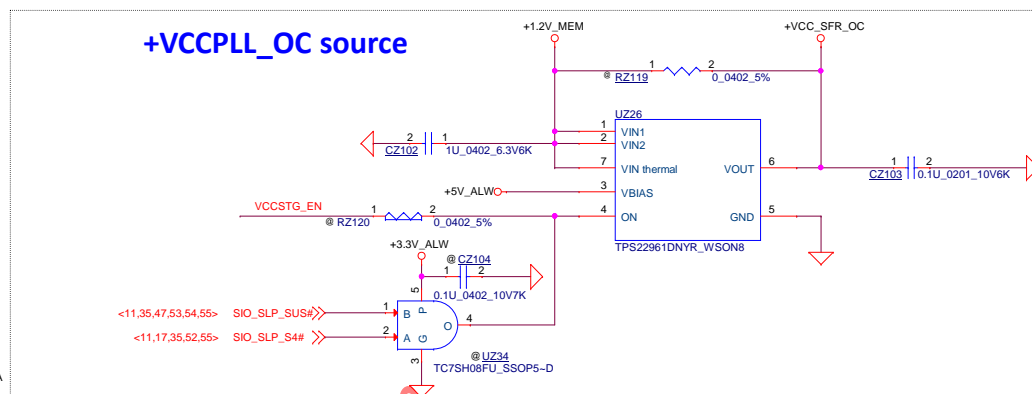
Reserve for soldering

+VCC_GTUS

GTU for SKYLAKE-U 2+3e



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+1.0V_VCCST source

UZ21

4.4mohm/6A
TR=12.5us@Vin=1.05V

TPS22961DNYR_WSON8

1 VIN1
2 VIN2
3 VIN thermal
4 VBIAS
5 GND
6 VOUT

1.0V_VCCST_C

PJP1

1 2
PAD-OPEN1x1m
CZ101 0.1uF_0201_10V6K

+1.0V_VCCST

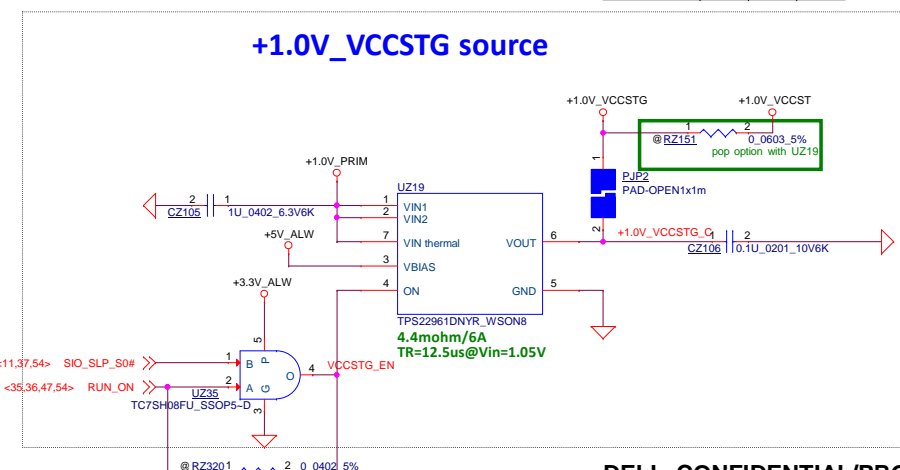
+1.0V_PRIM


+5V_ALW

CZ100 1uF_0402_6.3V6K

SIO_SLP_S4#

<11,17,35,52,55>



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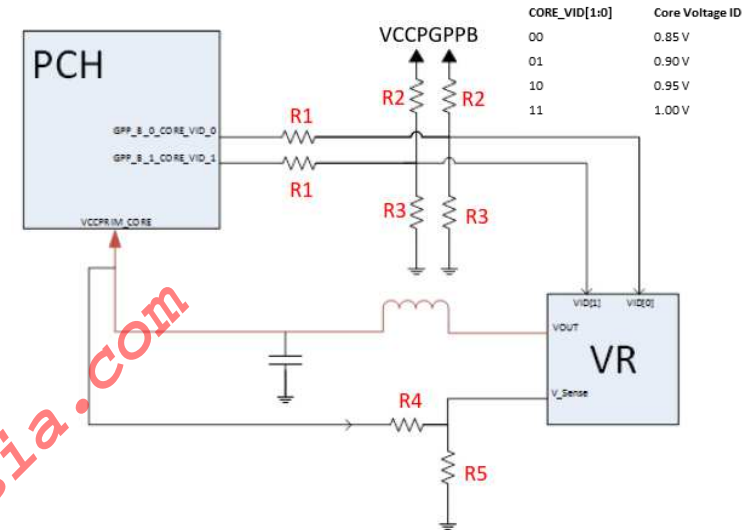
CPU (13/14)

LA-E071PRev
1.0

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Note1: VCCPRIM_CORE Implementat i on w t h PCH CORE_V D Reco mnendat i on

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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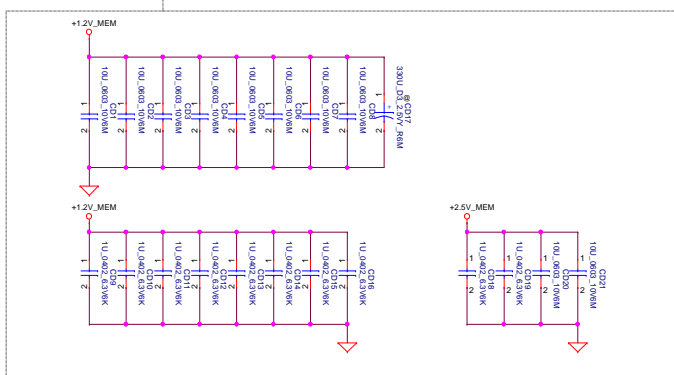


Title			CPU (14/14)	
Size			Document Number	Rev 1.0
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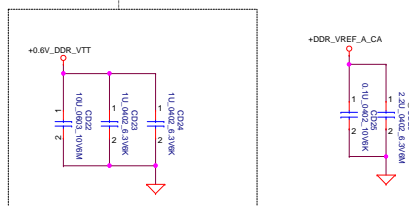
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<7> DDR_A_DQS#[0..7] <<>>
<7> DDR_A_D[0..63] <<>>
<7> DDR_A_DQS[0..7] <<>>
<7> DDR_A_MA[0..16] >>

Layout Note:
Place near JDIMM1

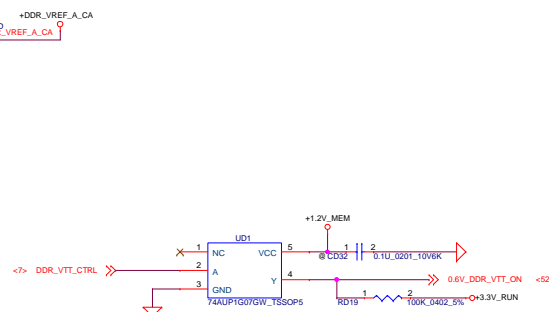
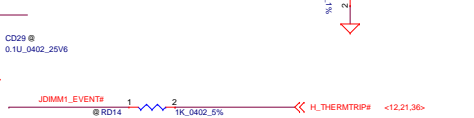
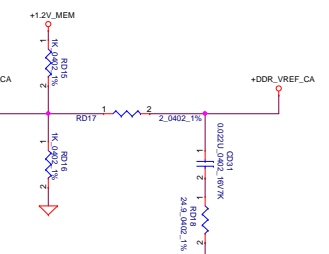
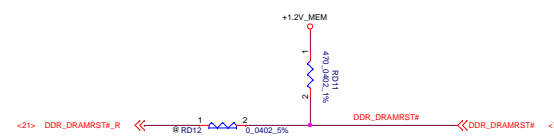
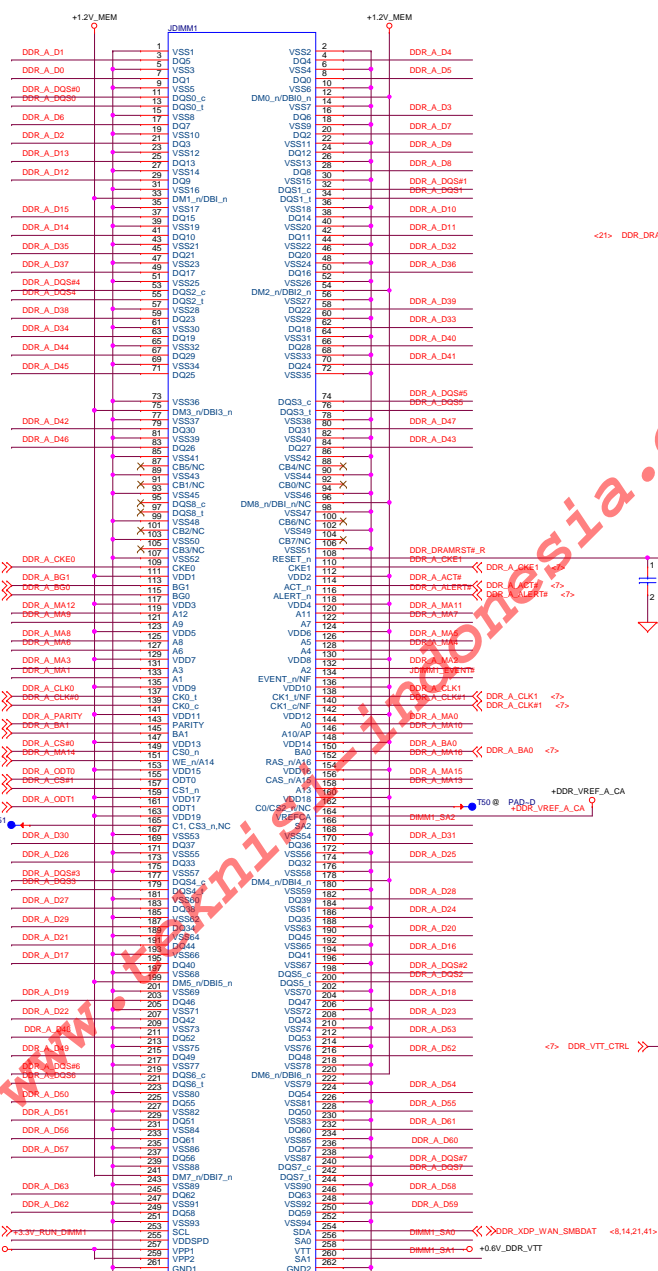
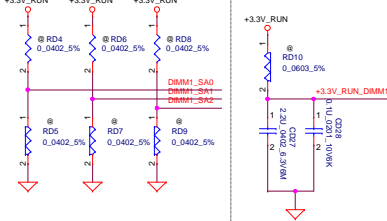


Layout Note:
Place near
JDIMM1.258



DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



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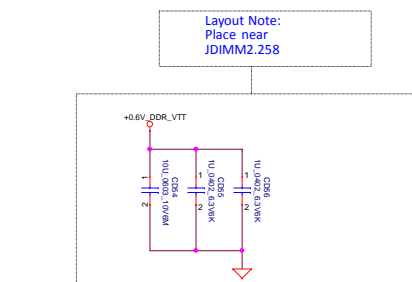
DDR4

LA-E071P

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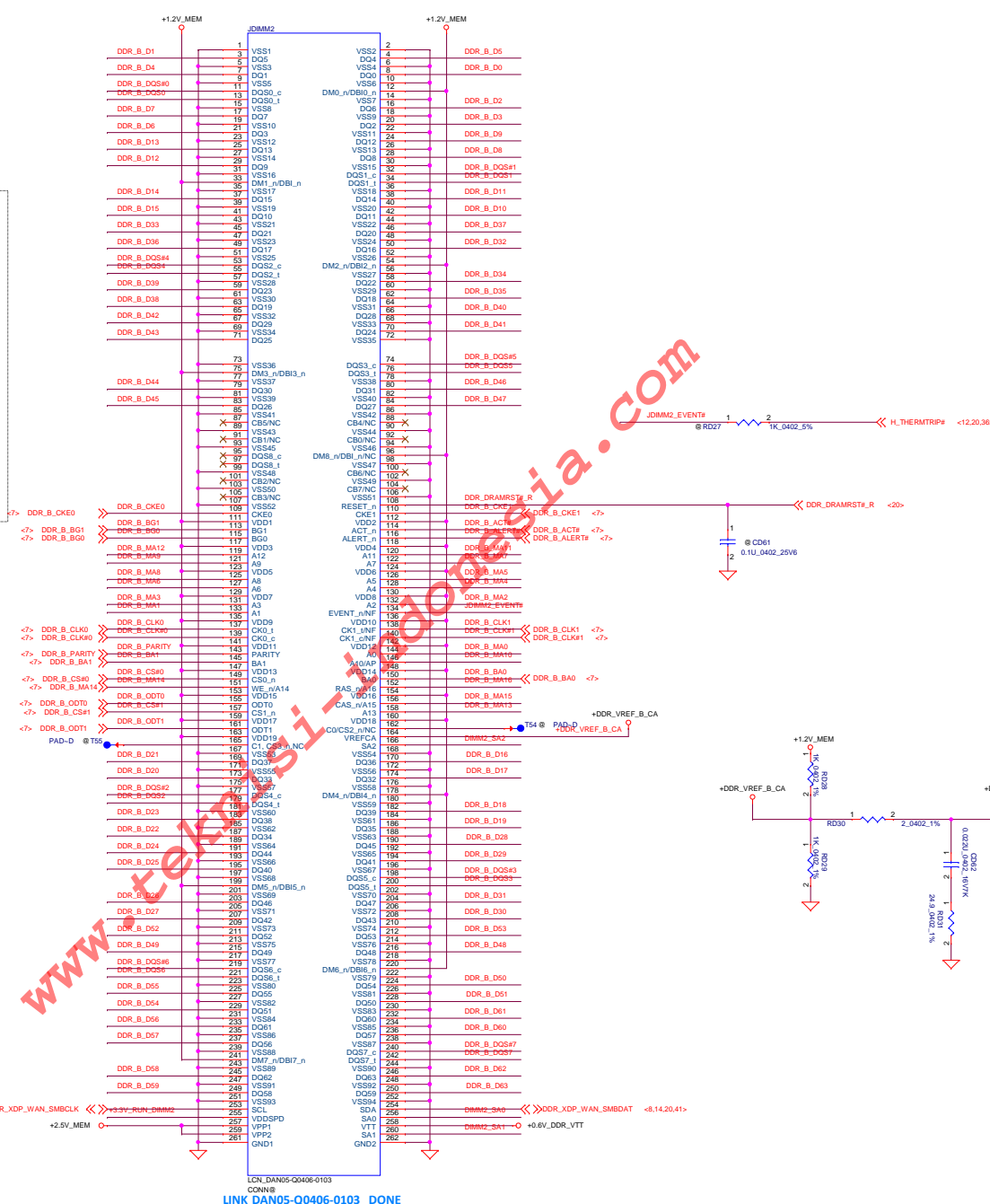
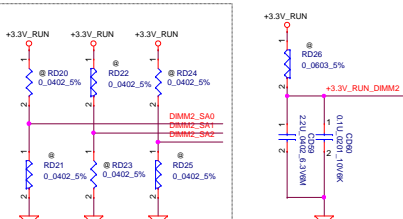


Note:
ear JDIMM2



DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
* DIMM3	0	1	0
DIMM4	1	1	0



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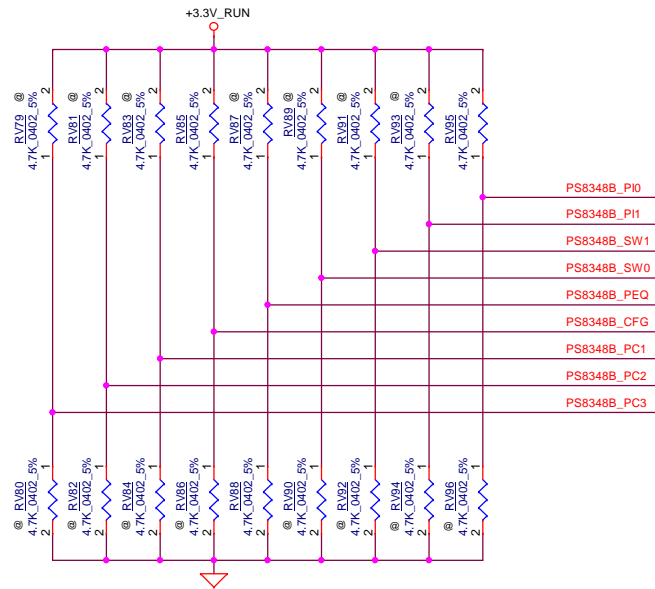
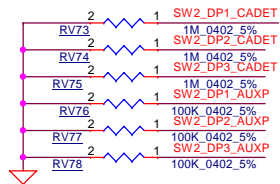
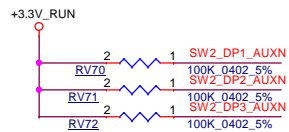
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DDR4

LA-E071P

LA-E071P
Date: Wednesday, November 30, 2016 Sheet 21 of 64



Internally tied to VDD33/2 3.3V I/O

PCx =
M: Port output configuration is set by link training (default)
H: Port output with fixed 800 mV and 0dB
L: Port output with fixed 400 mV and 0dB
x=1, 2, 3

Internally pull down ~150K 3.3V I/O
For Control Switching Mode (CFG = L):

[SW1,SW0] = [L,L], Port1 is selected (default)
[SW1,SW0] = [L,H], Port2 is selected
[SW1,SW0] = [H,L], Port3 is selected
[SW1,SW0] = [H,H], Port3 is selected

For Automatic Switching Mode (CFG = H):
[SW1,SW0] = [L,L], Port1 > Port2 > Port3 (default)

[SW1,SW0] = [L,H], Port1 > Port3 > Port2
[SW1,SW0] = [H,L], Port3 > Port2 > Port1
[SW1,SW0] = [H,H], Port3 > Port1 > Port2
[SW1,SW0] = [L,M], Port2 > Port1 > Port3
[SW1,SW0] = [M,M], Port2 > Port3 > Port1

PIO: Automatic EQ disable Internal pull down ~150K ohm 3.3V I/O
PIO = L: Automatic EQ enable (default)
H: Automatic EQ disable

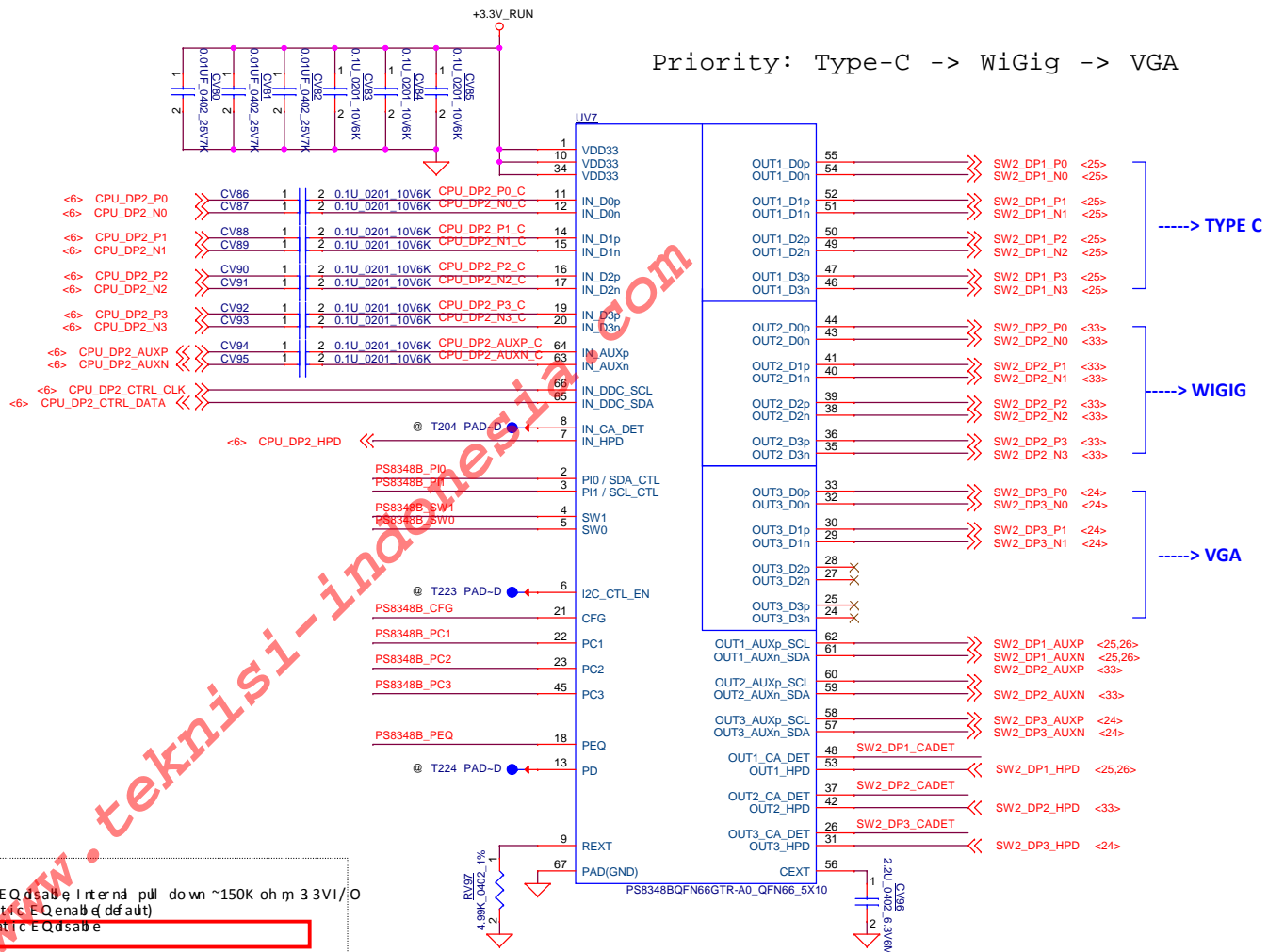
Internally tied to VDD33/2 3.3V I/O

PEQ =

M: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
L: LLEQ, compensate channel loss up to 8.5dB @ HBR2

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Priority: Type-C -> WiGig -> VGA

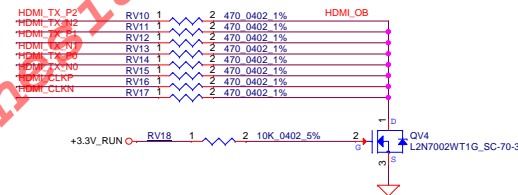
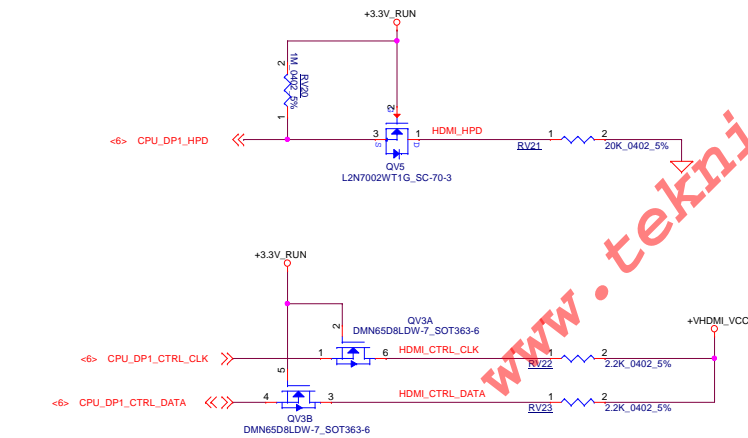


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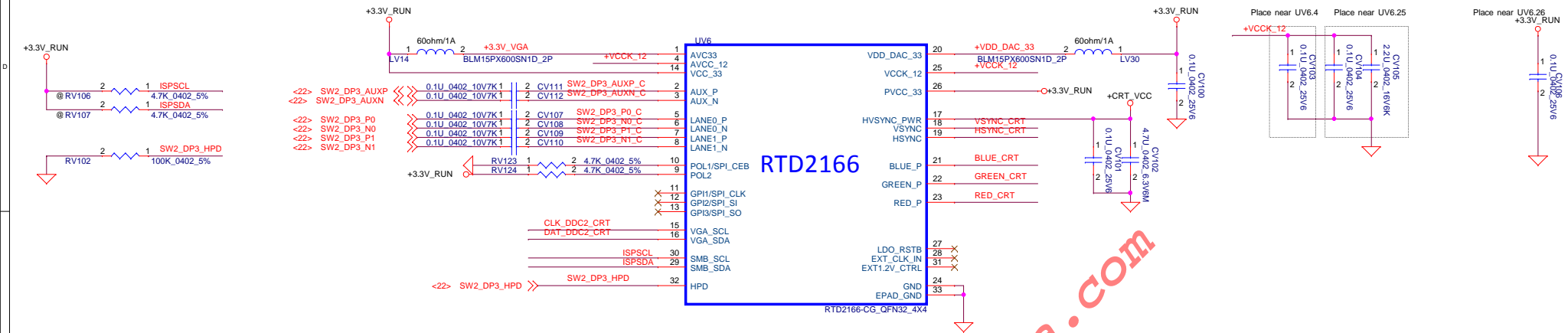


HDMI connector

LINK AHDM0046-P002A DONE

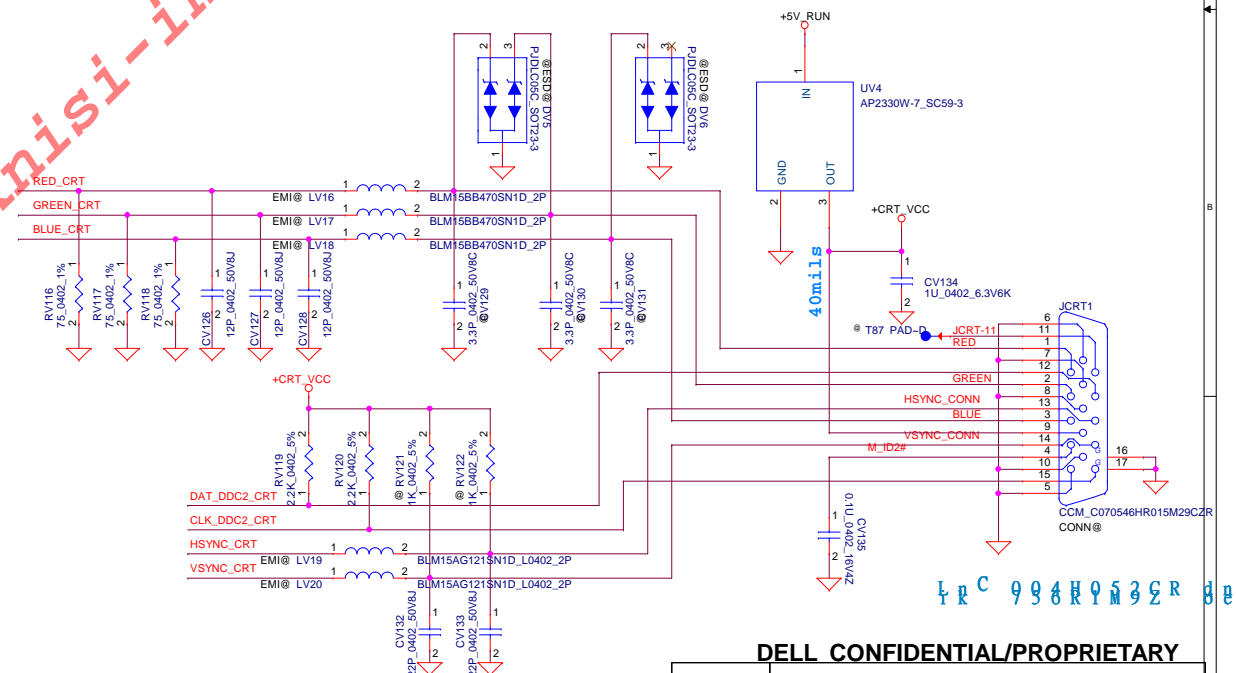
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For Breckenridge 12/14/15
For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM



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DP to VGA & VGA Conn

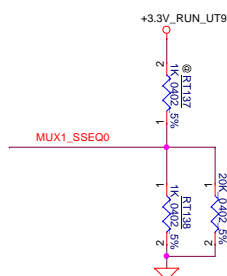
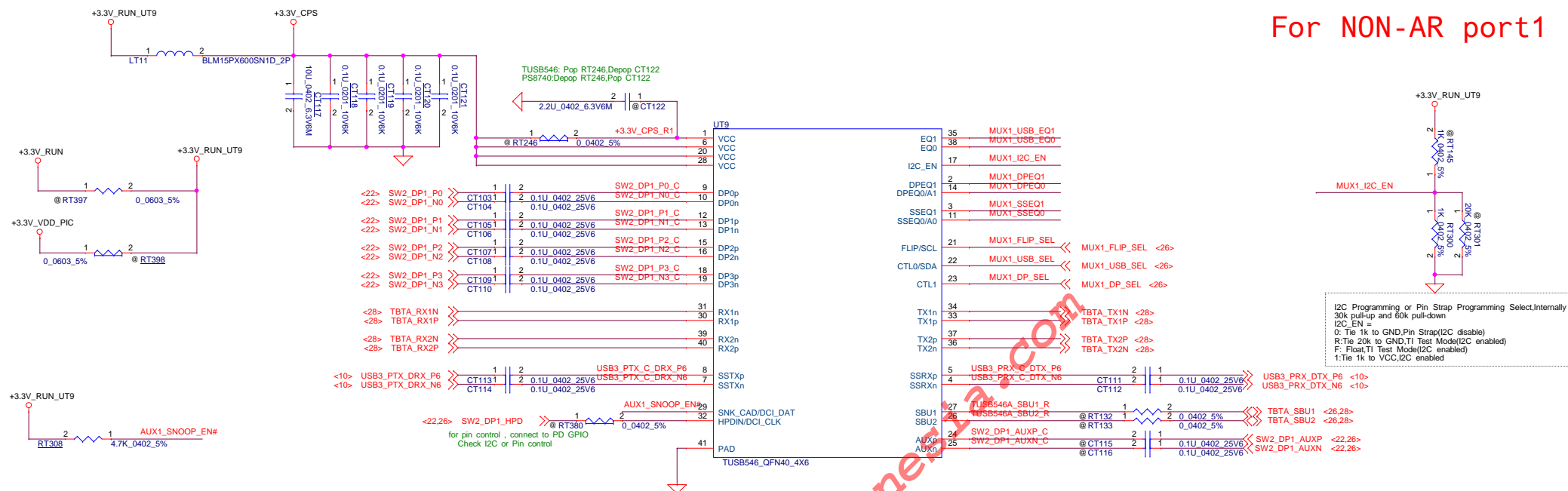
LA-E071P

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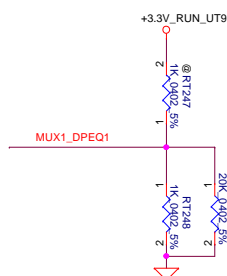
Date: Wednesday, November 30, 2016 Sheet 24 of 64

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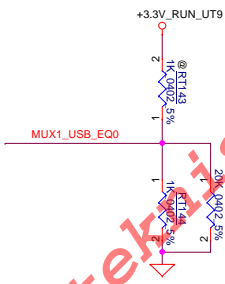
For NON-AR port1



Set the USB receiver equalizer gain for upstream facing
SSTXP/N, internally 30k pull-up and 60k pull-down
SSEQ =
0: Tie 1k to GND
R: Tie 20k to GND
F: Float
1: Tie 1k to VCC



Select the DisplayPort receiver equalizer gain ,Internally
30k pull-up and 60k pull-down
DPEQ =
0: Tie 1k to GND
R:Tie 20k to GND
F: Float
1:Tie 1k to VCC



Set the USB receiver equalizer gain for downstream facing RX1 and RX2 when USB utilized, internally 30k pull-up and 60k pull-down

USB_EQ =

0: Tie 1k to GND
1: Tie 20k to GND
2: Float
3: Tie 1k to VCC

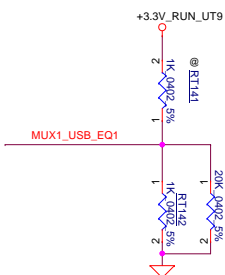
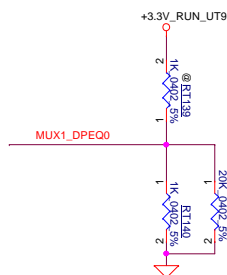
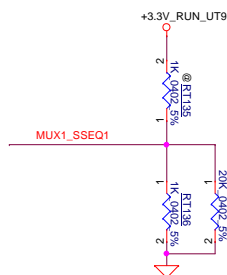


Table 8-7 TUSB546 Receiver Equalization GPIO Control

USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @5GHz (dB)	SSE1 pin Level	SSE0 pin Level	EQ GAIN @5GHz (dB)	DPE1 pin Level	DPE0 pin Level	EQ GAIN @5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

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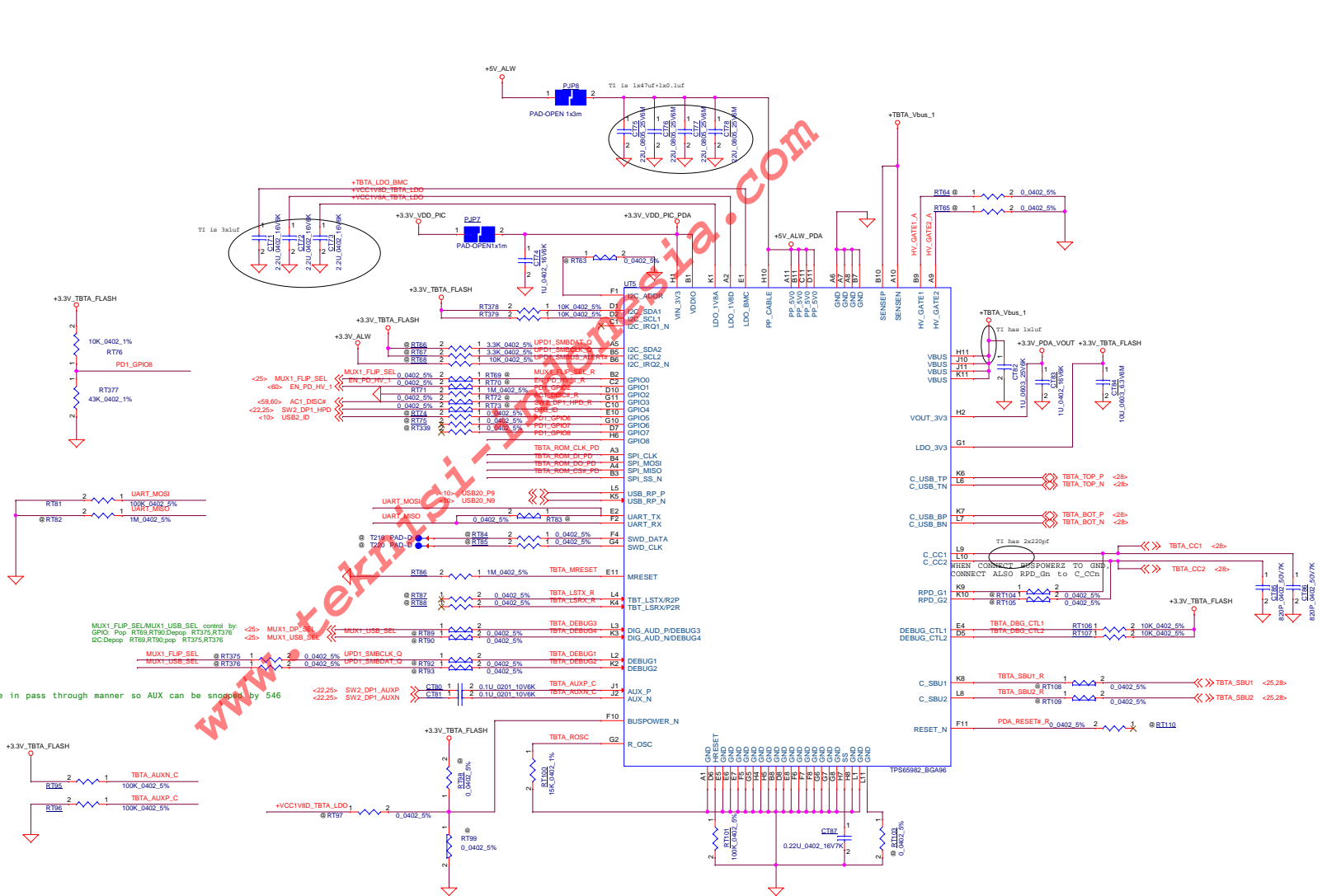
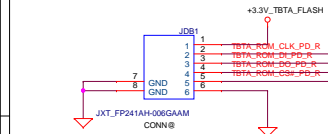
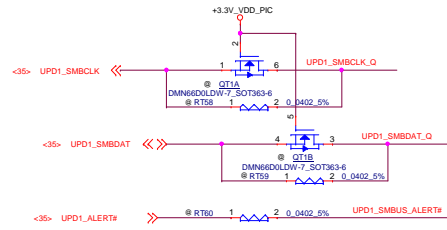
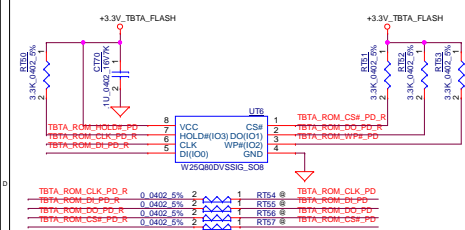
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Title **DP/USB3 Repeater SW TUSB546**

LA-E071P

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For NON-AR port1



DIV = R2/(R1+R2)		Factory Divide Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	<p>UFP only</p> <p>5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>TI VID supported</p>
0.10	0.18	1	<p>UFP only</p> <p>5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes -Sink, C and D pin configurations -TI VID supported</p>
0.20	0.28	2	<p>UFP only</p> <p>5V @3.0A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>TI VID supported</p>
0.30	0.38	3	<p>UFP only</p> <p>5V @3.0A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes -Sink, C and D pin configurations -TI VID supported</p>
0.40	0.48	4	<p>DRP</p> <p>5V @0.9-3.0A Sink capability</p> <p>5V @3.0A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes not supported</p> <p>TI VID supported</p> <p>Accepts data and power role swaps, but does not initiate.</p>
0.50	0.58	5	<p>DRP</p> <p>5V @0.9-3.0A Sink capability</p> <p>5V @3.0A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes - Source, C, D, and E pin configurations.</p> <p>TI VID supported</p> <p>Accepts power role swaps but will not initiate.</p> <p>Accepts data role swaps to UFP and can initiate.</p>
0.60	0.68	6	<p>DRP</p> <p>5V @0.9-3.0A Sink capability</p> <p>5V @3.0A Source capability</p> <p>TBT Alternate Modes not supported</p> <p>DisplayPort Alternate Modes - Source, C, D, and E pin configurations.</p> <p>TI VID supported</p> <p>Accepts power role swaps but will not initiate.</p> <p>Accepts data role swaps to DRP and can initiate.</p>
0.70	1.00	7	<p>Infinite boot retry from Flash to Host IF cycles.</p>

Route in pass through manner so AUX can be snooped by 546

Link TPS65982D (from SA00009W200 to SA00009W210) 08/04

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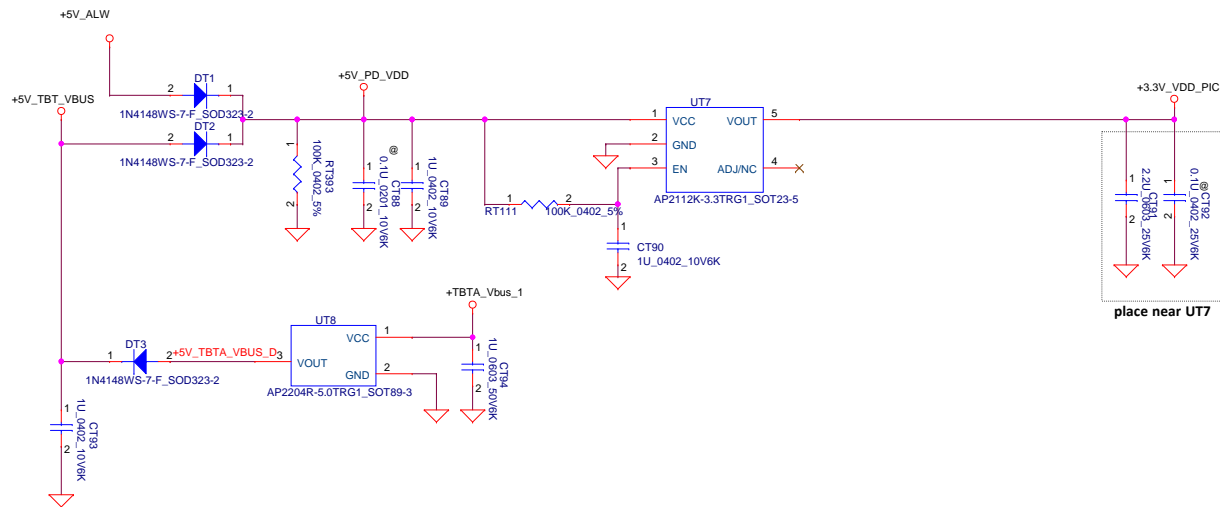
[Type C]PD Controller TI

LA-E071P

Rev		
1.0		

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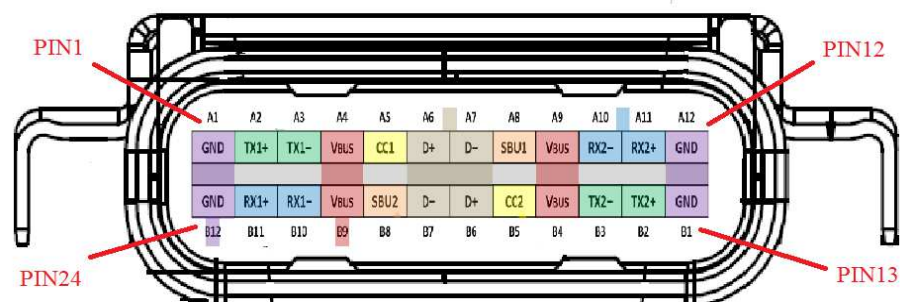
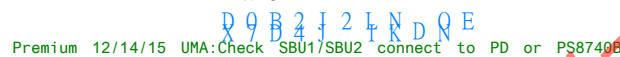
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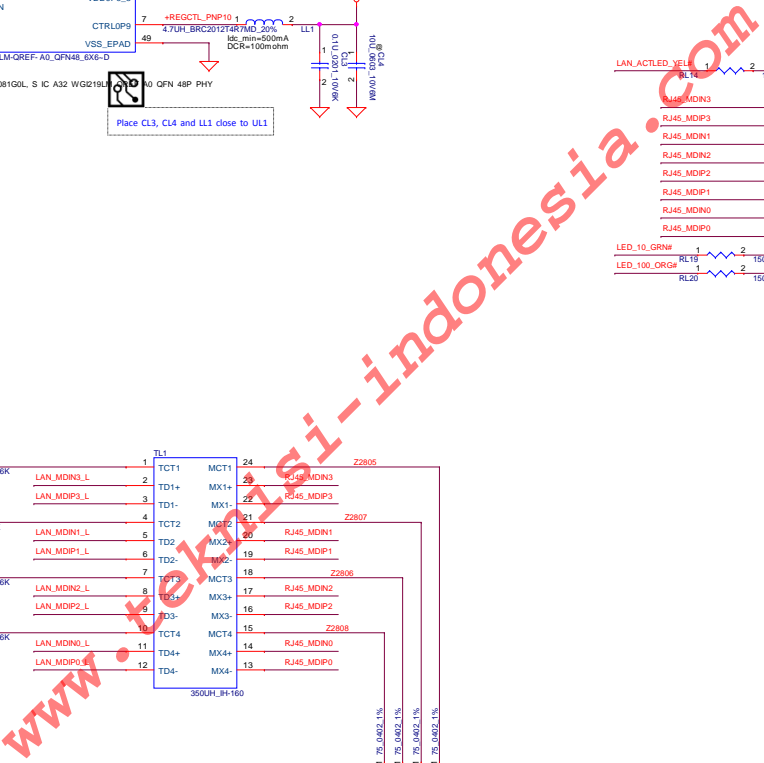
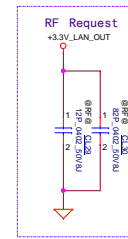


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[Type C]PD Power			
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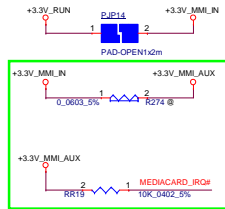
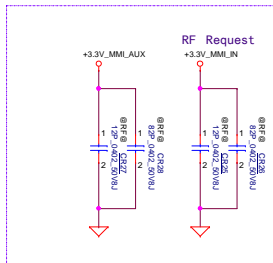
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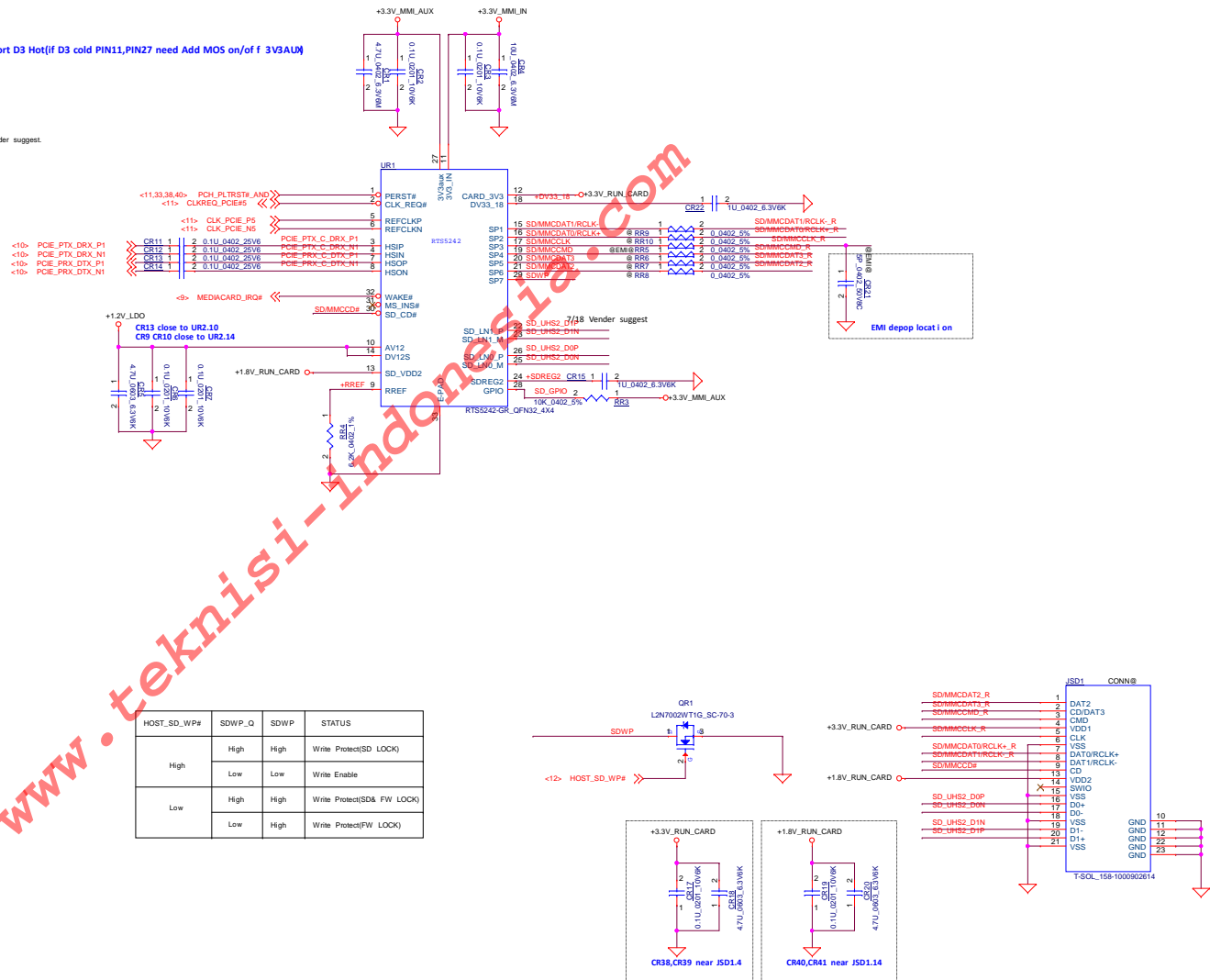


For PCIE Interface



support D3 Hot (if D3 cold PIN11, PIN27 need Add MOS on/of 3V3AUX)

7/18 Vender suggest.



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Card Reader RTS5242

LA-E071P


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NO SUPPORT

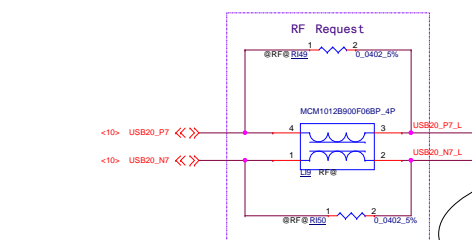
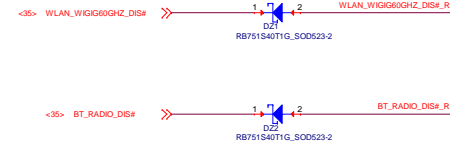
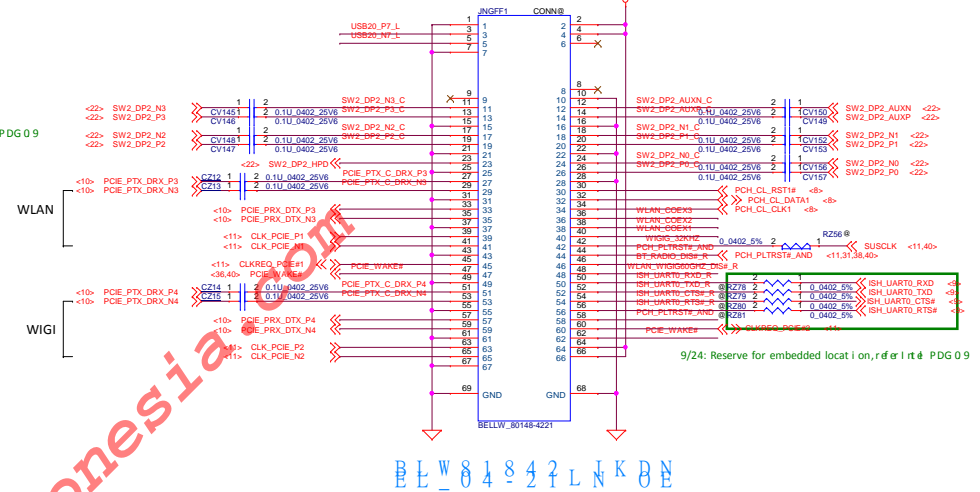
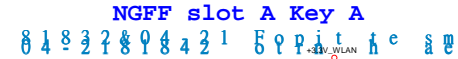
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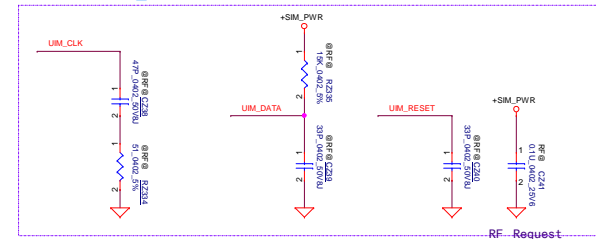
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Title			PCIE REPEATER for M.2 3042		
Size			Document Number		
			LA-E071P		
Date			Rev		
Wednesday, November 30, 2016			1.0		
Sheet			32 of 64		

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for no AR, Breckenridge 12/14/15 UMA/Steamboat



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				



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NGFF Card

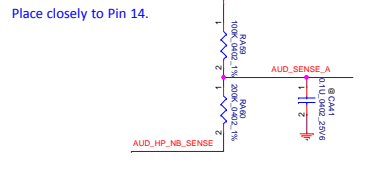
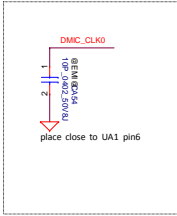
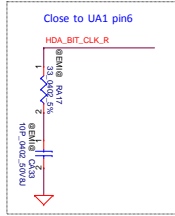
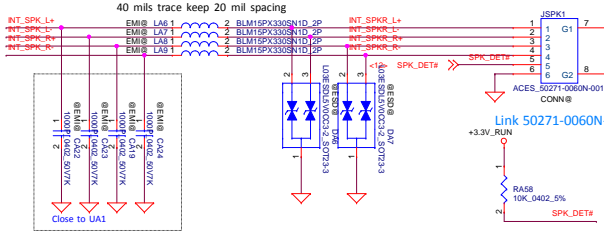
LA-E071P

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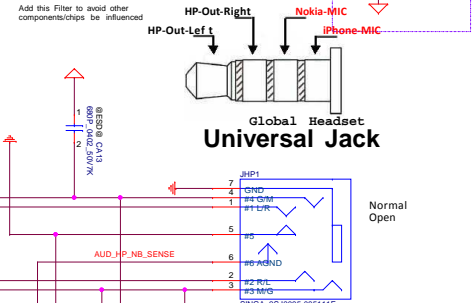
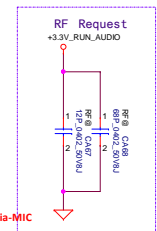
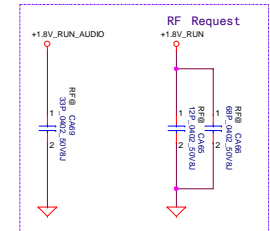
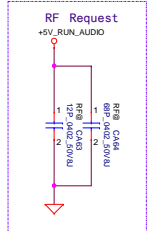
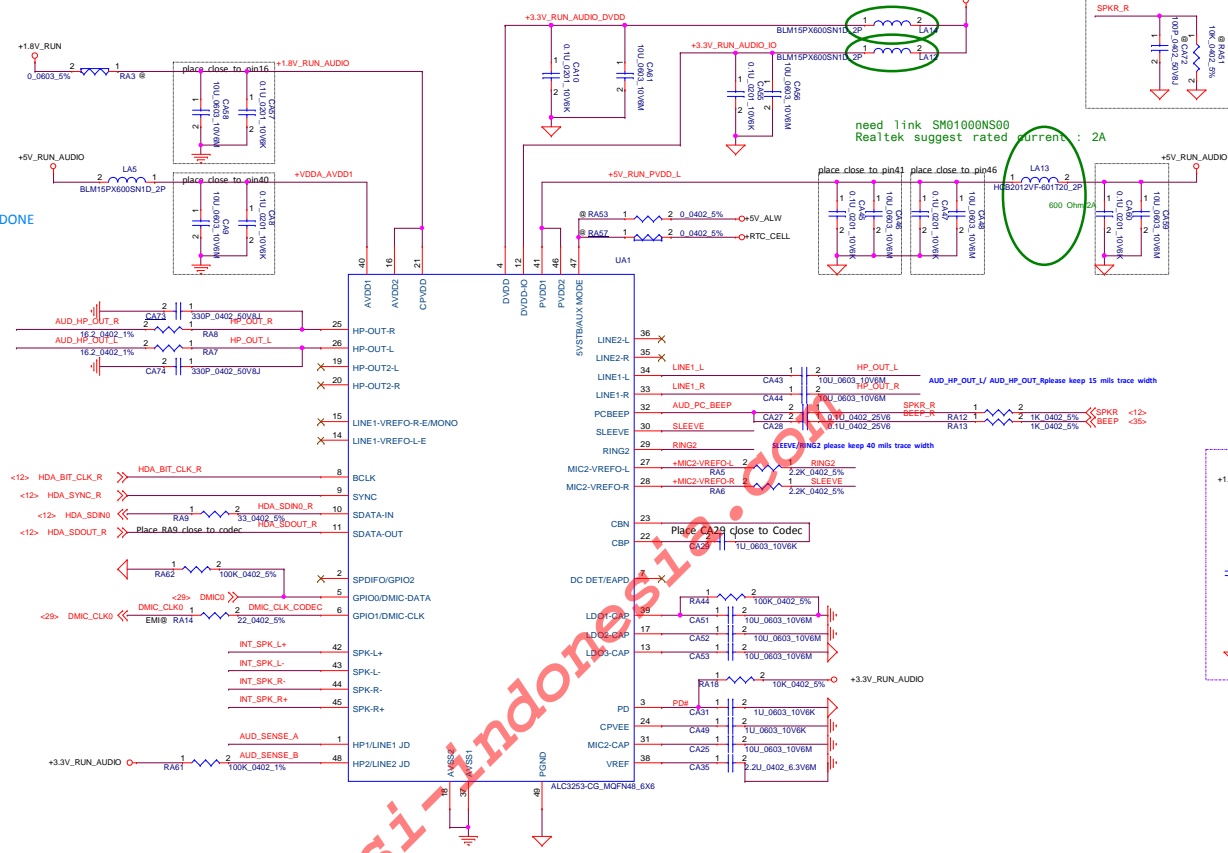
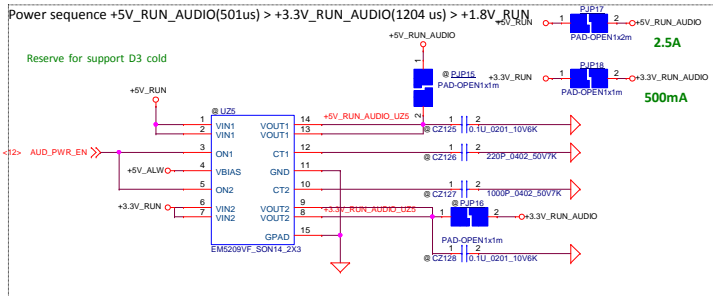
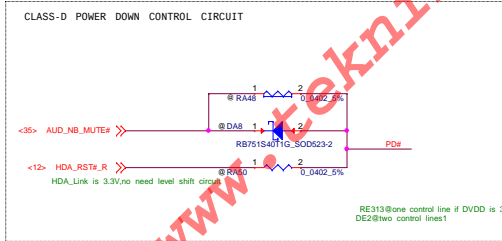
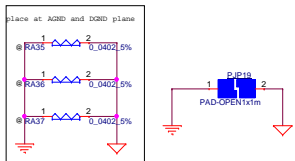
1W x 1ch, 4ohm (Transducer spec is 80mm0.5Watt per unit, there are two transducer units in one speaker box)

Internal Speakers Header

40 mils trace keep 20 mil spacing

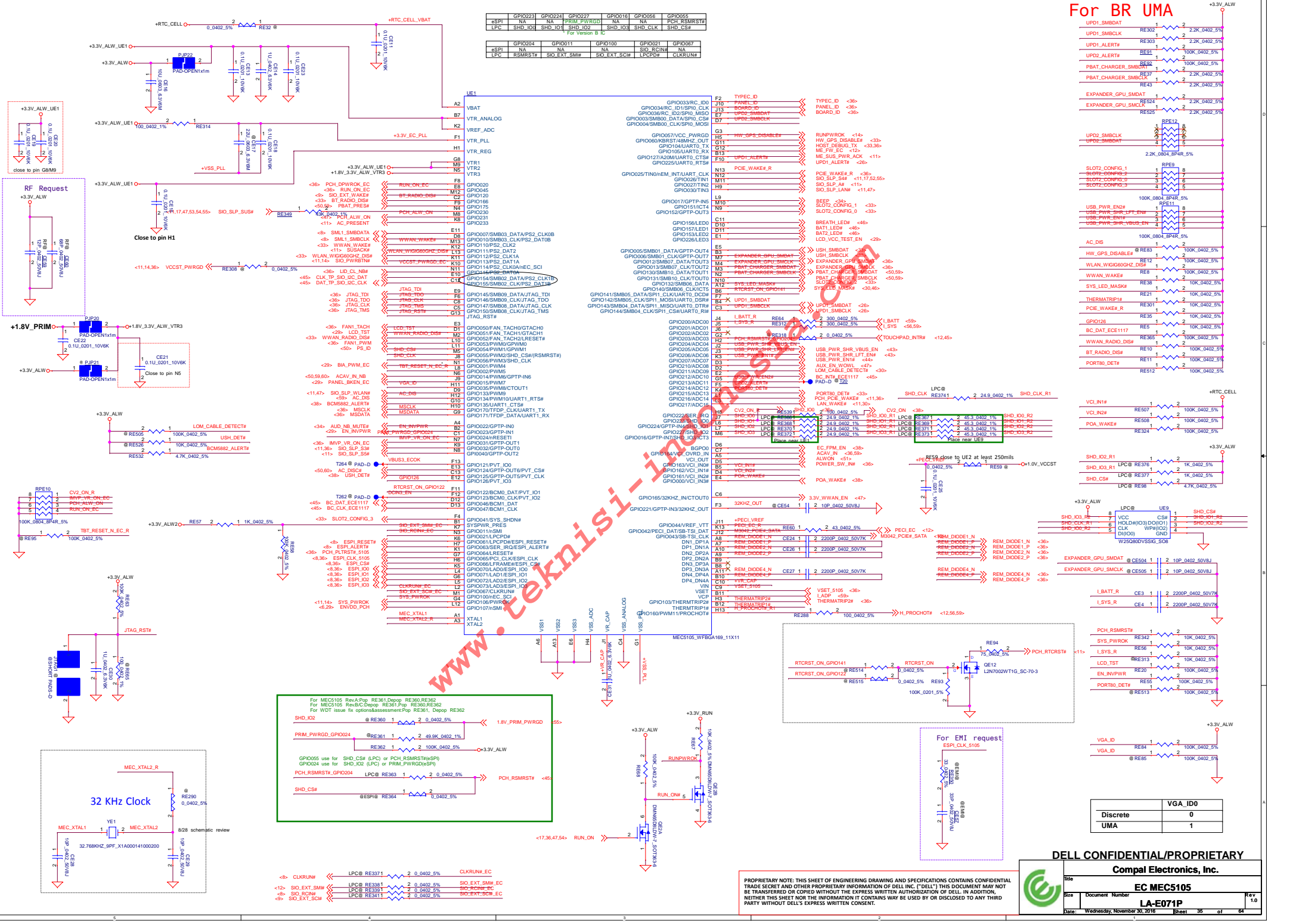


Add for solve pop noise and detect issue

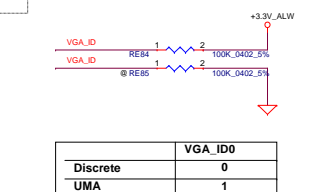
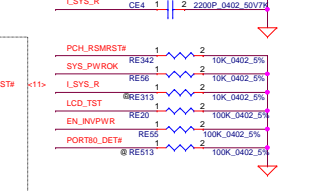
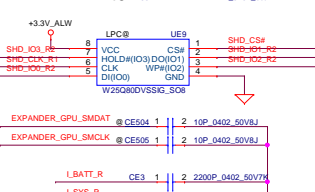
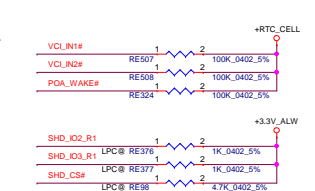
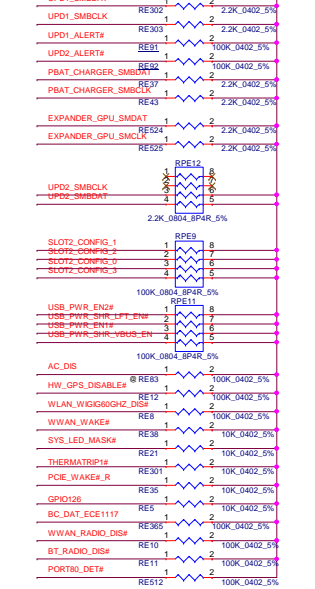


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For BR UMA

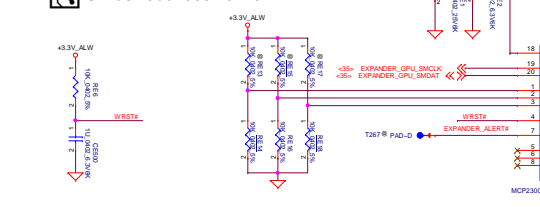


Discrete		UMA
0		1

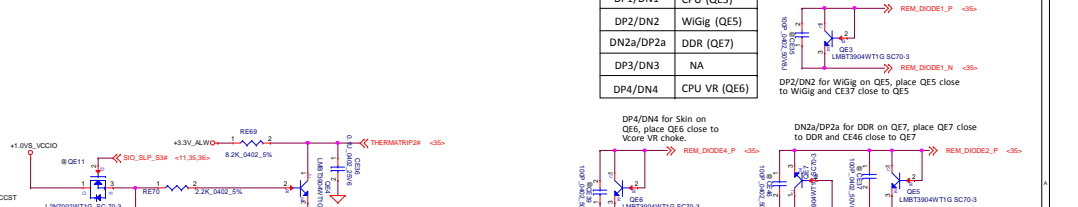
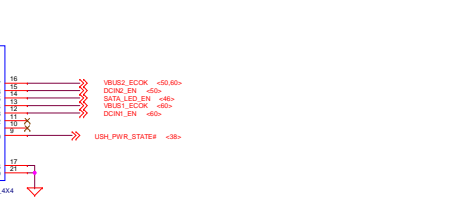
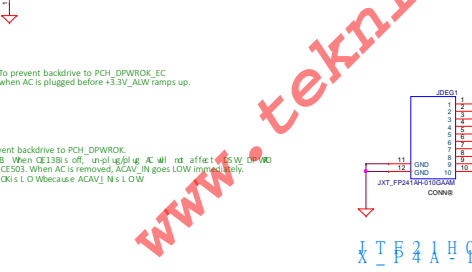
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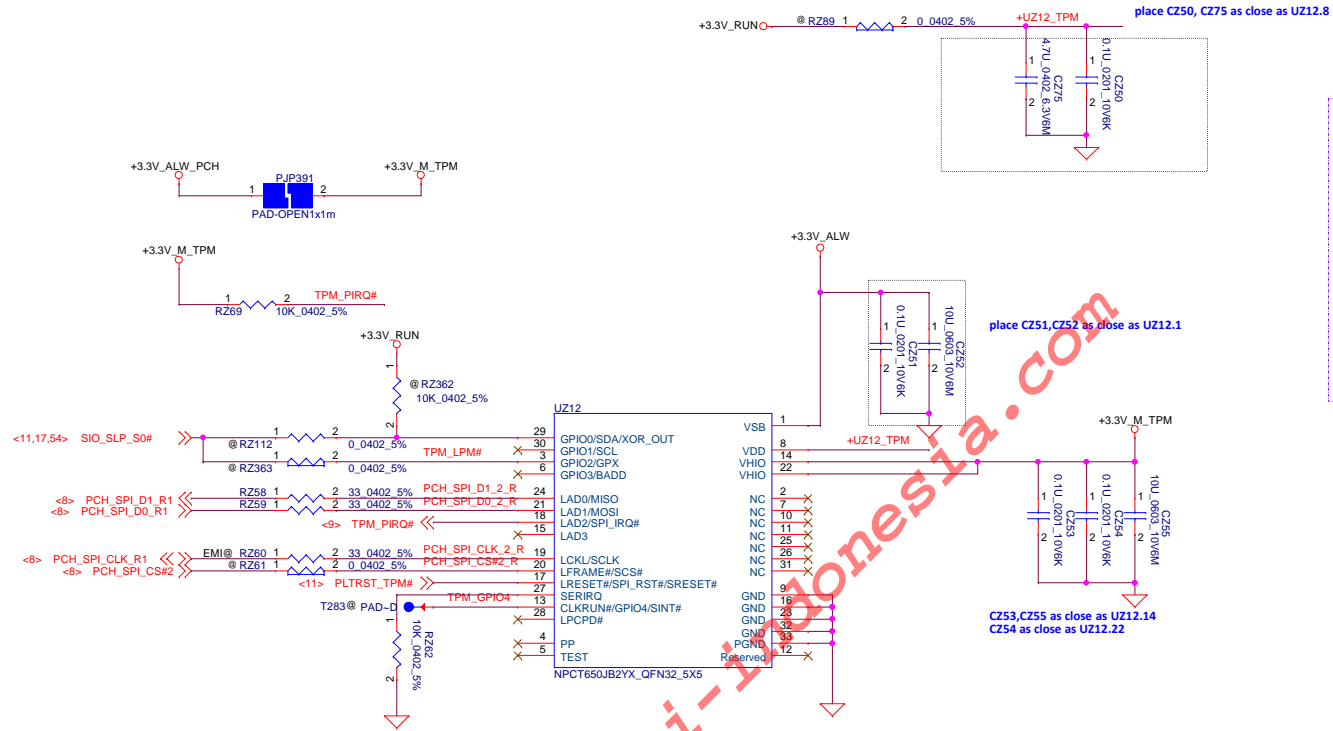
EC MEC5105		Rev 1.0
Date:	Wednesday, November 30, 2016	Sheet 35 of 64

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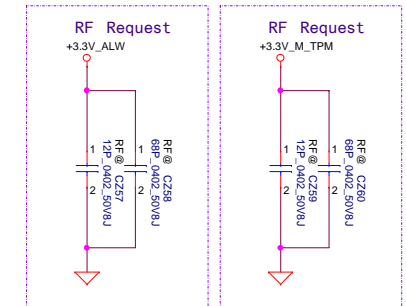
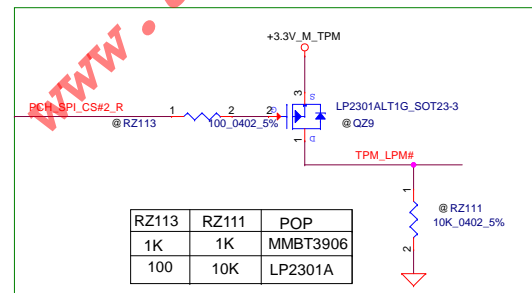
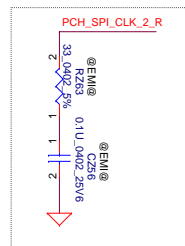


The timing diagram shows a digital signal trace for PCH_DPWROK <t1>. The signal transitions from low to high at approximately 0.8 ns after the start of the observation window. A label 'PCH_DPWROK <t1>' is placed near the rising edge.





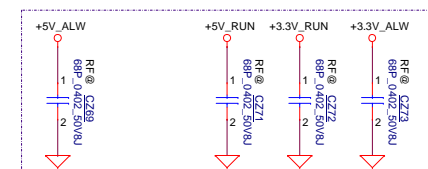
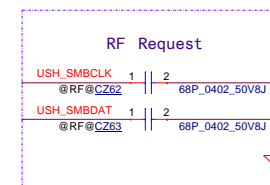
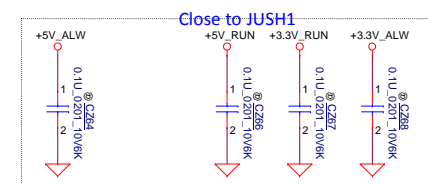
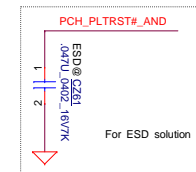
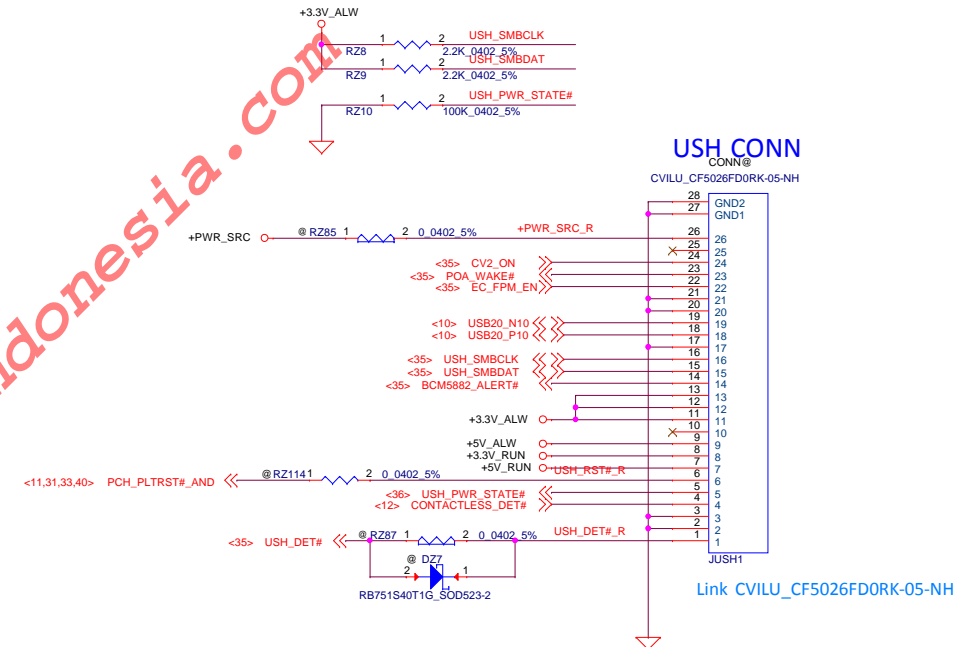
JB2YX change to VB2YX 09/08



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Title			
USH & TPM			
Size	Document Number	Rev 1.0	
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USH & TPM

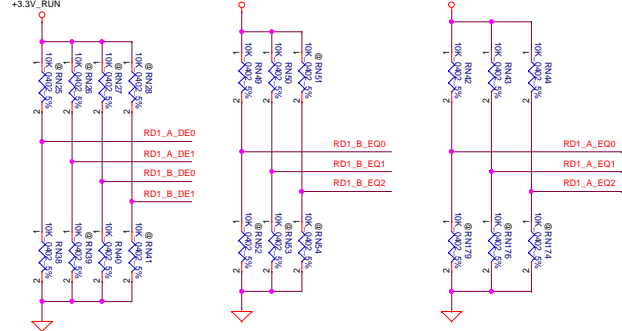
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	PCIe/SATA Redriver for 2280
Brekenridge12	Need
Brekenridge14U UMA	Need
Brekenridge14U DSC	Need
Brekenridge15U UMA	Need
Brekenridge15U DSC	Need
Steamboat12	No need
Steamboat14	Need
Kirkwood12&13	Check

FWD	Function
0	Normal mode(default)
1	power down mode

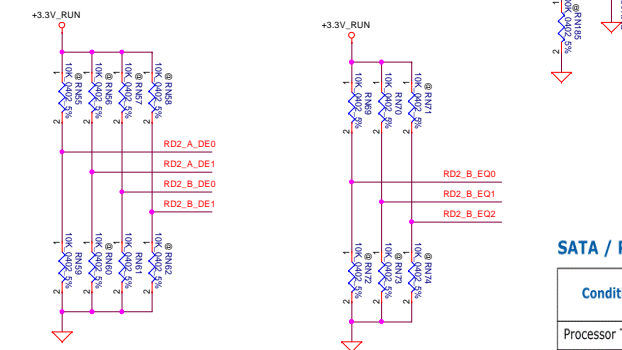


Programmable output de-emphasis level setting for channel A
A_DE0: internally pulled up at ~150K;
A_DE1 internally pulled down at ~150K
[A_DE1A_DE0] ==
HL: -7.5dB
LH: -3.5dB (default)
HH: -6dB

Programmable output de-emphasis level setting for channel B
B_DE0: internally pulled up at ~150K;
B_DE1 internally pulled down at ~150K
[B_DE1B_DE0] ==
HL: -7.5dB
LH: -3.5dB (default)
HH: -6dB

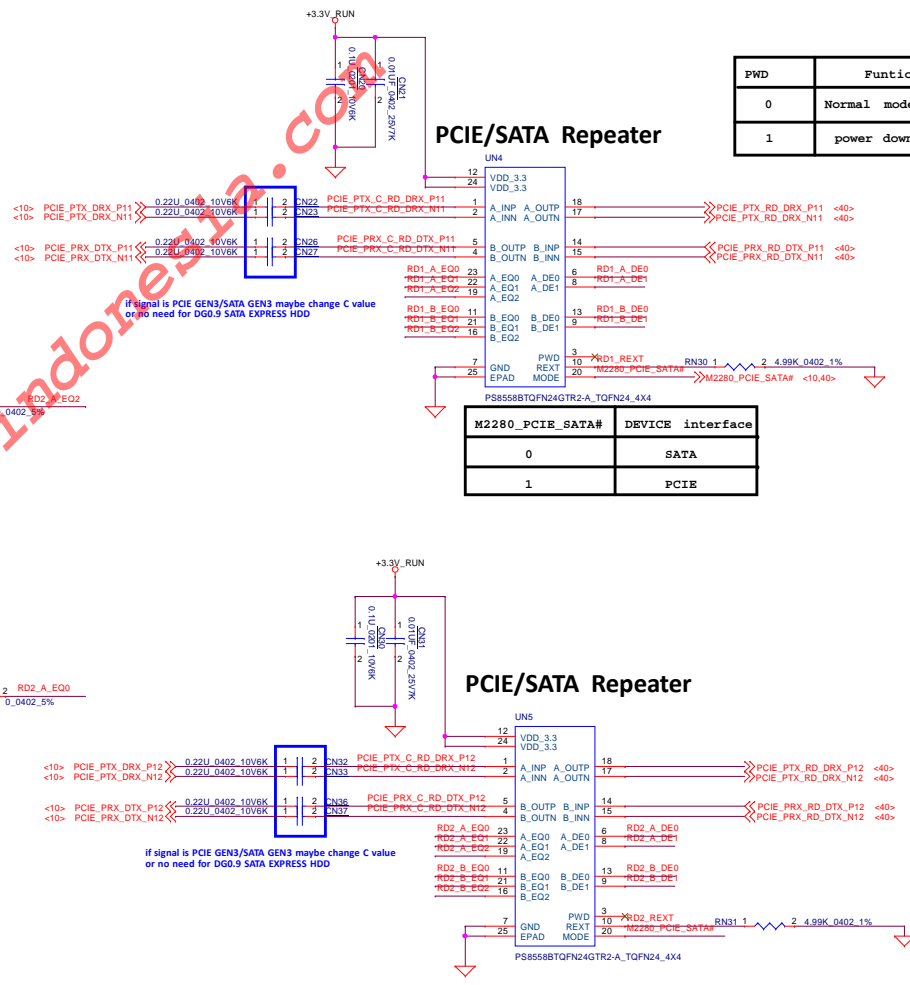
Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K
[A_EQ2A_EQ1A_EQ0] ==
LLL: For channel loss up to 17dB (default)
LHL: For channel loss up to 14dB
HLL: For channel loss up to 19dB
HHL: For channel loss up to 21dB
LHH: For channel loss up to 18dB
HHH: For channel loss up to 16dB
HHH: For channel loss up to 20dB

Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K
[B_EQ2B_EQ1B_EQ0] ==
LLL: For channel loss up to 17dB (default)
LHL: For channel loss up to 14dB
HLL: For channel loss up to 19dB
HHL: For channel loss up to 21dB
LHH: For channel loss up to 18dB
HHH: For channel loss up to 16dB
HHH: For channel loss up to 20dB



SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

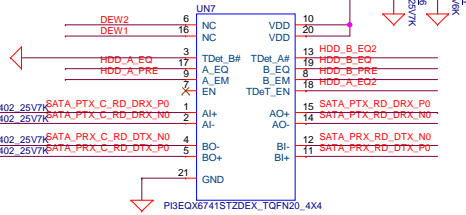


PCIe/SATA Repeater

M2280_PCIE_SATA#	DEVICE interface
0	SATA
1	PCIe

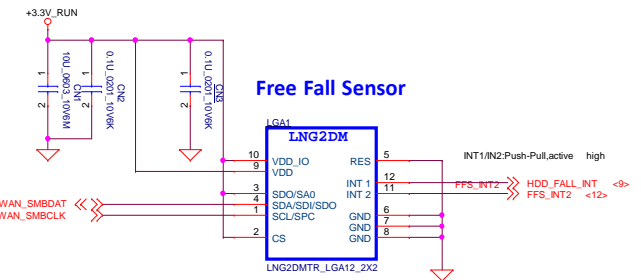
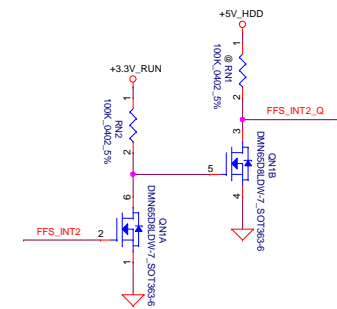
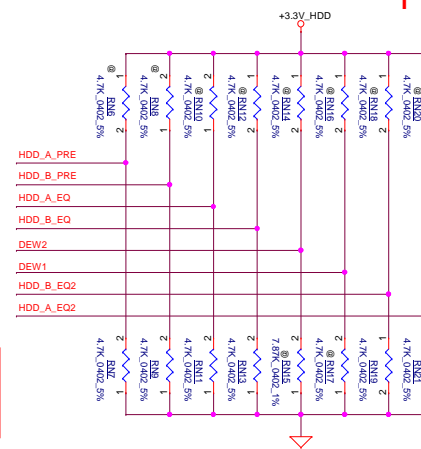
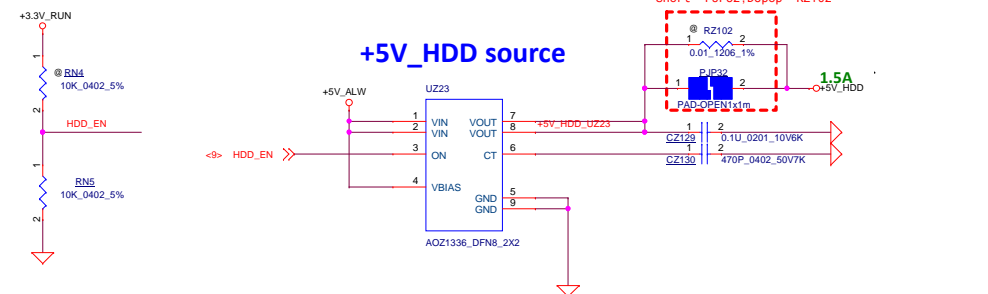
	pin_3	pin_6	pin_9	pin_16	pin_17
Pericom	TDet_B#	N_P	TDet_A#	C _D	TDet_EN
TI	N_D	B_W	N_D	B_W	N_D
Parade	N_D	B_W	B_EQ2	B_W	A_EQ2

SATA Repeater

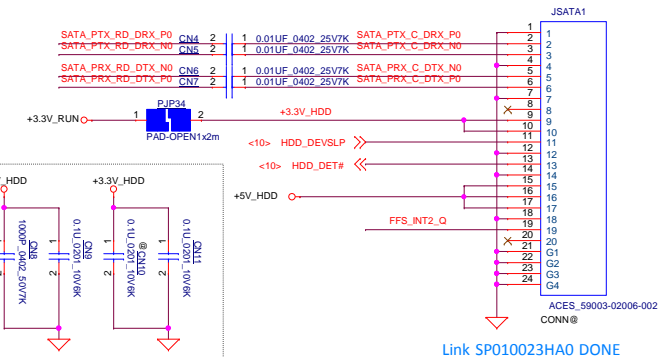
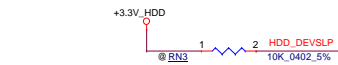


	HDD_A_EQ	HDD_B_EQ	HDD_A_EQ2	HDD_B_EQ2	DEW1	DEW2	HDD_A_PRE	HDD_B_PRE
Pericom PI3EQX6741ST	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC	NC	PD (RN7)	PD (RN9)
TI SN75LVCP601	PD (RN11)	NC	PD (RN21)	PD (RN19)	NC (IPU)	NC (IPU)	PH (RN6)	PH (RN8)
Parade PS8527C	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC (1/2 VDD)	PD (RN15)	NC (1/2 VDD)	NC (1/2 VDD)

			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
2nd	TI	0 NC 1	7dB 0dB 14dB	7dB 0dB 14dB	0 NC 1	0dB -4dB -2dB	0dB -4dB -2dB
3rd	Parade	EQ2 EQ1 (M = VDD/2)	2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	0 M 0 M 0 1 M M M 0 M 1 1 M 1 0 1 1	0 M 0 M 0 1 M M M 0 M 1 1 M 1 0 1 1	0dB -3.5dB -1.5dB

*Pd & Pr is V & E
& t f g

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)



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SATA Repeater&HDD CONN	
LA-E071P	
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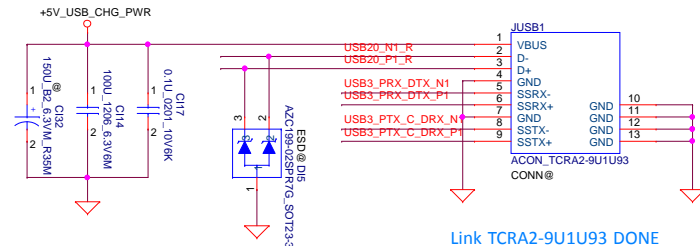
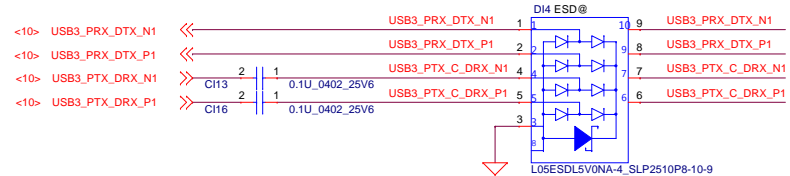
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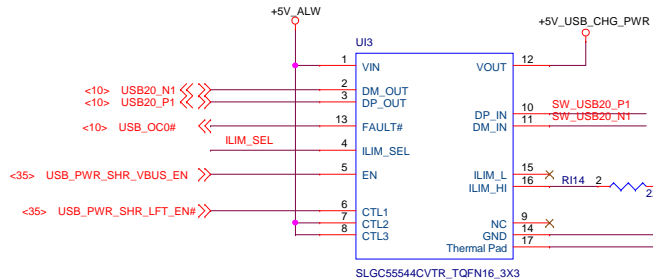
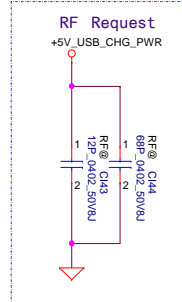
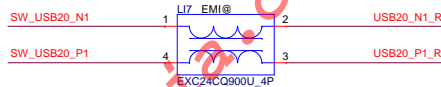
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Size	Document Number	Rev
	LA-E071P	1.0
Date: Wednesday, November 30, 2016		
Sheet 42 of 64		

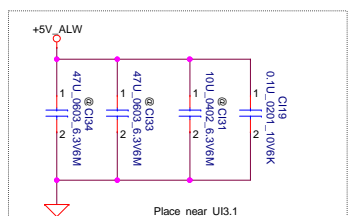
For w/o Repeater



Link TCRA2-9U1U93 DONE



Link Seligro SA000097E10 Done
MAIN:SLGC55544CVTR



Place near UI3.1

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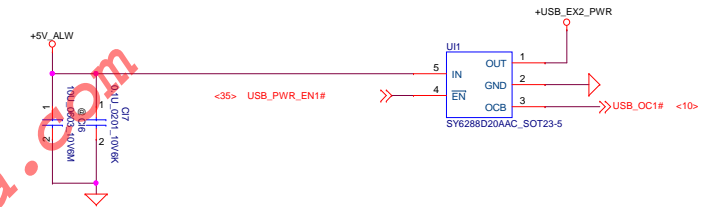
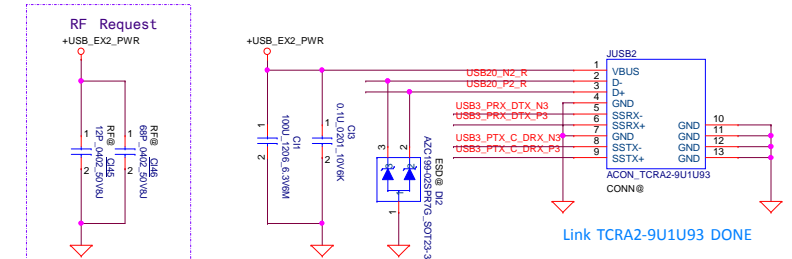
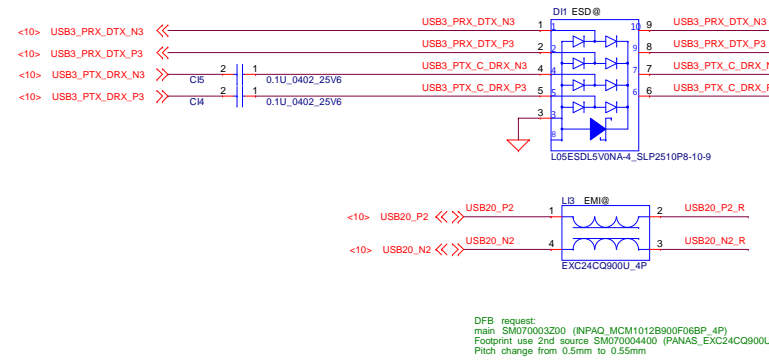
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Title			JUSB1+PS
Size	Document Number	Rev	
		1.0	
Date:	Wednesday, November 30, 2016	Sheet	43 of 64

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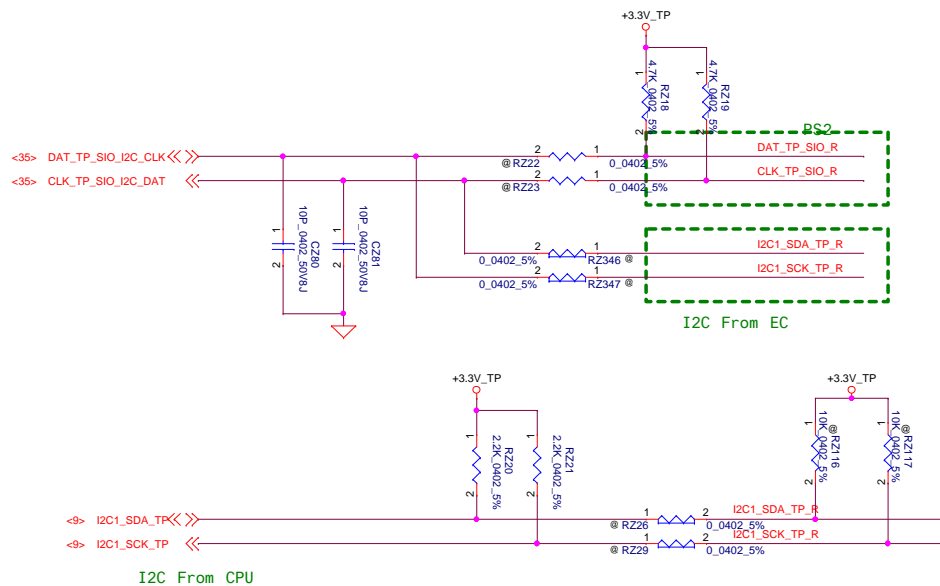


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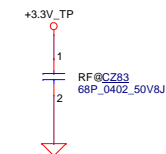
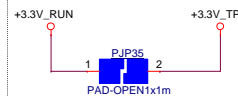
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Touch Pad



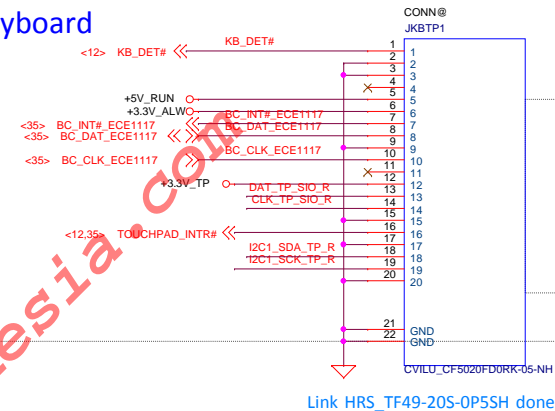
Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



RF Request

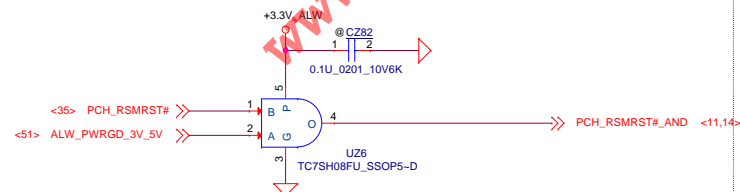
KB_DET#	1	2	
RF@ C284			68P_0402_50VBJ
BC_INT#_ECE1117	1	2	
@RF@ C285			68P_0402_50VBJ
BC_DAT_ECE1117	1	2	
@RF@ C286			68P_0402_50VBJ
BC_CLK_ECE1117	1	2	
@RF@ C287			68P_0402_50VBJ
DAT_TP_SIO_R	1	2	
@RF@ C288			68P_0402_50VBJ
CLK_TP_SIO_R	1	2	
@RF@ C289			68P_0402_50VBJ

Keyboard



+3.3V_TP +3.3V_ALW +5V_RUN
 1 1 1
 2 2 2
 0.1u 0.201 10V/6K
 0.1u 0.201 10V/6K
 0.1u 0.201 10V/6K
 Place close to JKB

RSMRST circuit



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Keyboard

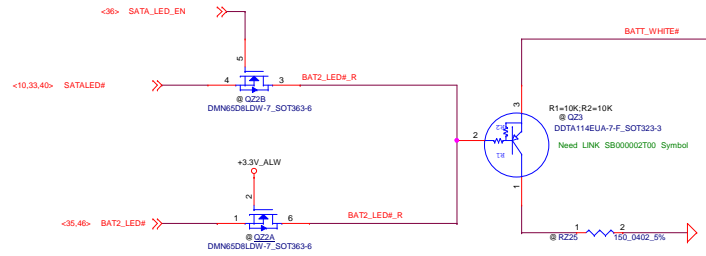
LA-E071P

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	LA-E071P	1.0
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Battery LED

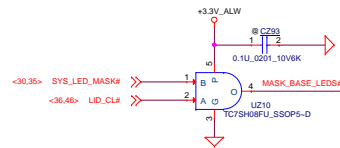
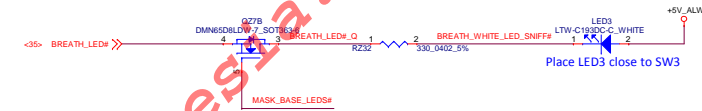
HDD LED MUX

means EC can switch battery white led and HDD LED by hot key - Fn+F1

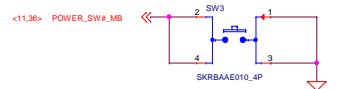


Breath LED

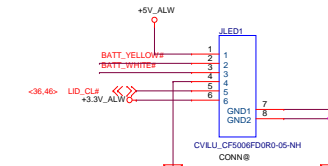
LED PIN change to SC50000FL00 from SC50000BA00



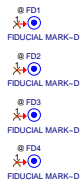
POWER & INSTANT ON SWITCH



LED board CONN

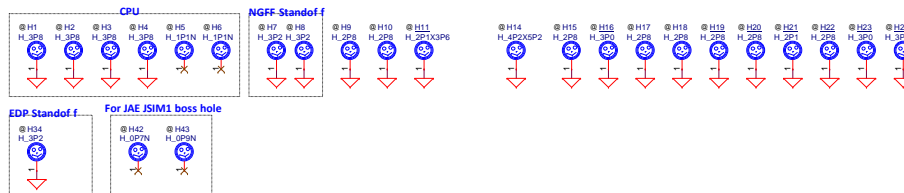


Fiducial Mark



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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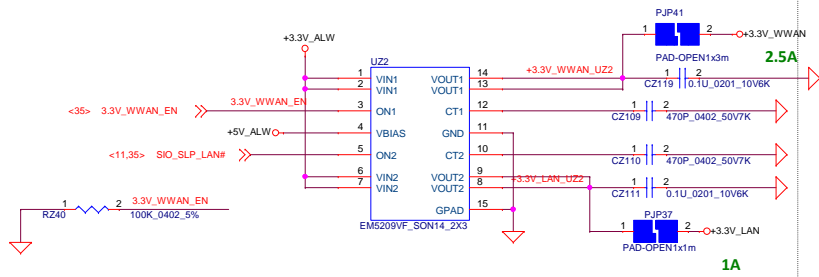
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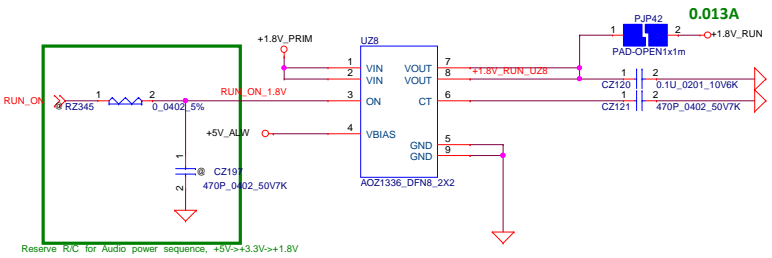
Rev	Document Number	Sheet	of	64
1.0	PAD, LED	46	of	64
Date:	Wednesday, November 30, 2016			

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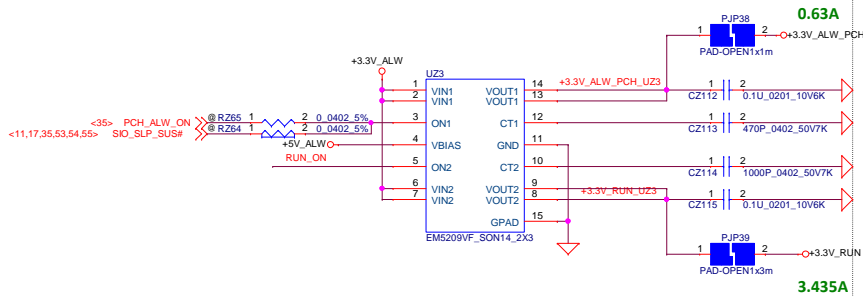
+3.3V_WWAN/+3.3V_LAN source



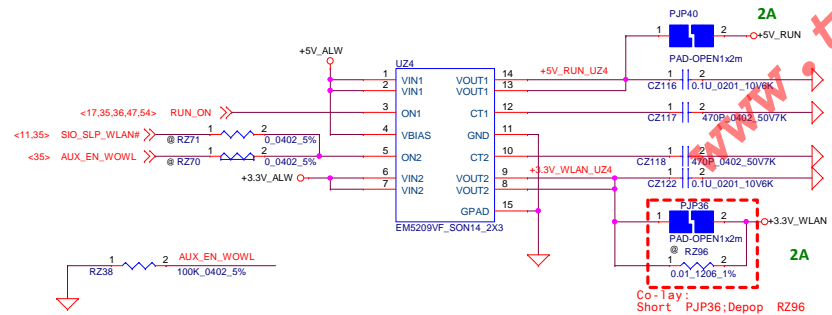
+1.8V_RUN source



+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WLAN source

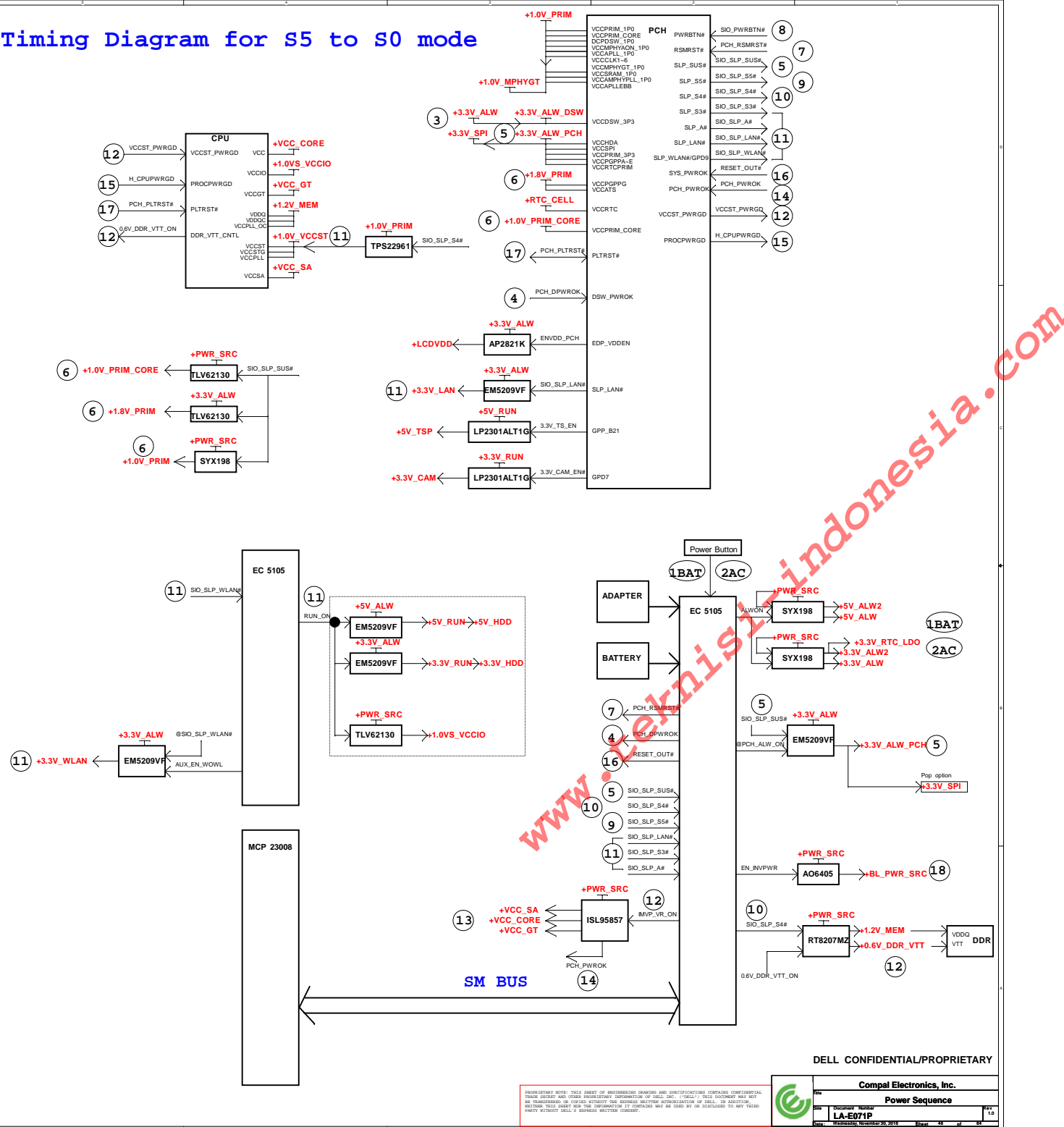


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Timing Diagram for S5 to S0 mode



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1

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil	Delay time(ps/inch)	25 ± 2.5 ohm single-end	35 ± 3.5 ohm single-end	39 ± 3.9 ohm single-end	43 ± 4.3 ohm single-end	45 ± 4.5 ohm single-end	48 ± 4.8 ohm single-end	50 ± 5 ohm single-end	52 ± 5.2 ohm single-end	50 ± 5 ohm Diff.	70 ± 7 ohm Diff.	75 ± 7.5 ohm Diff.	80 ± 8 ohm Diff.	83 ± 8.3 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	88 ± 8.8 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	100 ± 10 ohm Diff.	Ref	100 ± 10 ohm Diff.	Ref	90 ± 9 ohm Diff.	Ref			
			SolderMask	IT-158	0.5																																
			Add Plating																																		
			Copper foil	0.5oz+plating	1.6	149.18	13.4	8	6.8	9.5	5	4.4	4	3.7	13.5X	8.65.2	5.54.5	4.43.7	3.93.5	4.1	3.73.8				4.9	4.6.7	3.74.7	3.3	3.54.2	3.59.3	L.2	3.93.5	no Ref	10%	L.3		
1	Top	3.8	Prepreg	1080	2.6		24.98	34.95	39.05	43.06	45.2	48.08	50.23	52	無法檢測	69.98	75	79.85	82.85	84.88	85.11				86.12	90.04	89.99	89.92	89.96	100.02		99.28		89.48			
		3.7	Copper foil	4mil	3.87										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46	SE 50	SE 50	SE 52	SE 48										
2	GND	3.7	Prepreg	2116H	4.1	161.77	11.4	6.8	5.8	4.7	4.3	3.7	3.5	3.3	11.4X	5.63.5	4.83.8	4.34.1	3.93.5	3.53.4	3.33.3	3.74.1	4.34.2	3.54.3	3.54.3	3.34.3	3.74.7		3.93.5	L2/L4	9.5%	no Ref					
		3.7	Copper foil	1oz	1.25		24.92	34.99	39.12	42.94	44.9	46.22	49.45	51.84	無法檢測	69.94	74.93	79.85	83.81	84.76	85.01	85.13	85.05	87.88	89.86	89.97	89.99				99.84		99.61				
		3.7	Copper foil	4mil	3.87										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48			SE 50	SE 50	SE 52										
5	IN 2	3.8	Prepreg	1080H x2 oz/PP2116HRC	4.2	166.76	15.5	9.3	7.7	6.5	5.8	5.2	4.6	4.4	15.5X	7.75	6.84.6	5.23.7	4.63.6	4.34.3	4.43.6	5.23.2			4.85.2	4.85.3	4.44.7			4.07.0	L.4/L.7	8.5%	no Ref				
		3.7	Copper foil	1oz	1.25		24.88	34.96	39.08	42.88	45.09	48.01	49.87	51.89	48.1	70.2	76.38	80.01	83.17	85.27	85.09	85.35			86.39	90.32	89.95			100.26		99.84		100.69			
		3.7	Copper foil	4mil	3.87										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46	SE 50	SE 50	SE 52	SE 48										
7	GND/PWR	3.8	Prepreg	2116H	4.1										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46	SE 50	SE 50	SE 52	SE 48										
		3.7	Copper foil	1oz	1.25		24.92	34.99	39.12	42.94	44.9	46.22	49.45	51.84	無法檢測	69.94	74.93	79.85	83.81	84.76	85.01	85.13	85.05	87.88	89.86	89.97	89.99				99.84		99.75				
		3.7	Copper foil	4mil	3.87										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46	SE 50	SE 50	SE 52	SE 48										
9	GND	3.8	Prepreg	1080	2.6										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46	SE 50	SE 50	SE 52	SE 48										
		3.7	Copper foil	0.5oz+plating	1.6		13.4	8	6.8	9.5	5	4.4	4	3.7	13.5X	8.65.2	5.54.5	4.43.7	3.93.5	4.1	3.73.8				4.9	4.6.7	3.74.7	3.3	3.54.2	3.59.3	L.9	3.93.5	no Ref				
			Add Plating												無法檢測	69.98	75	79.85	82.85	84.88	85.11				86.12	90.04	89.99	89.92	89.96	100.02		99.75					
			SolderMask	IT-158	0.5																																
Overall Thickness (1.2mm ± 10%)					47.68000																																
					1.211072																																

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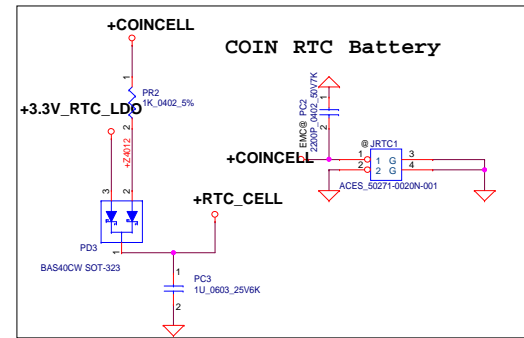
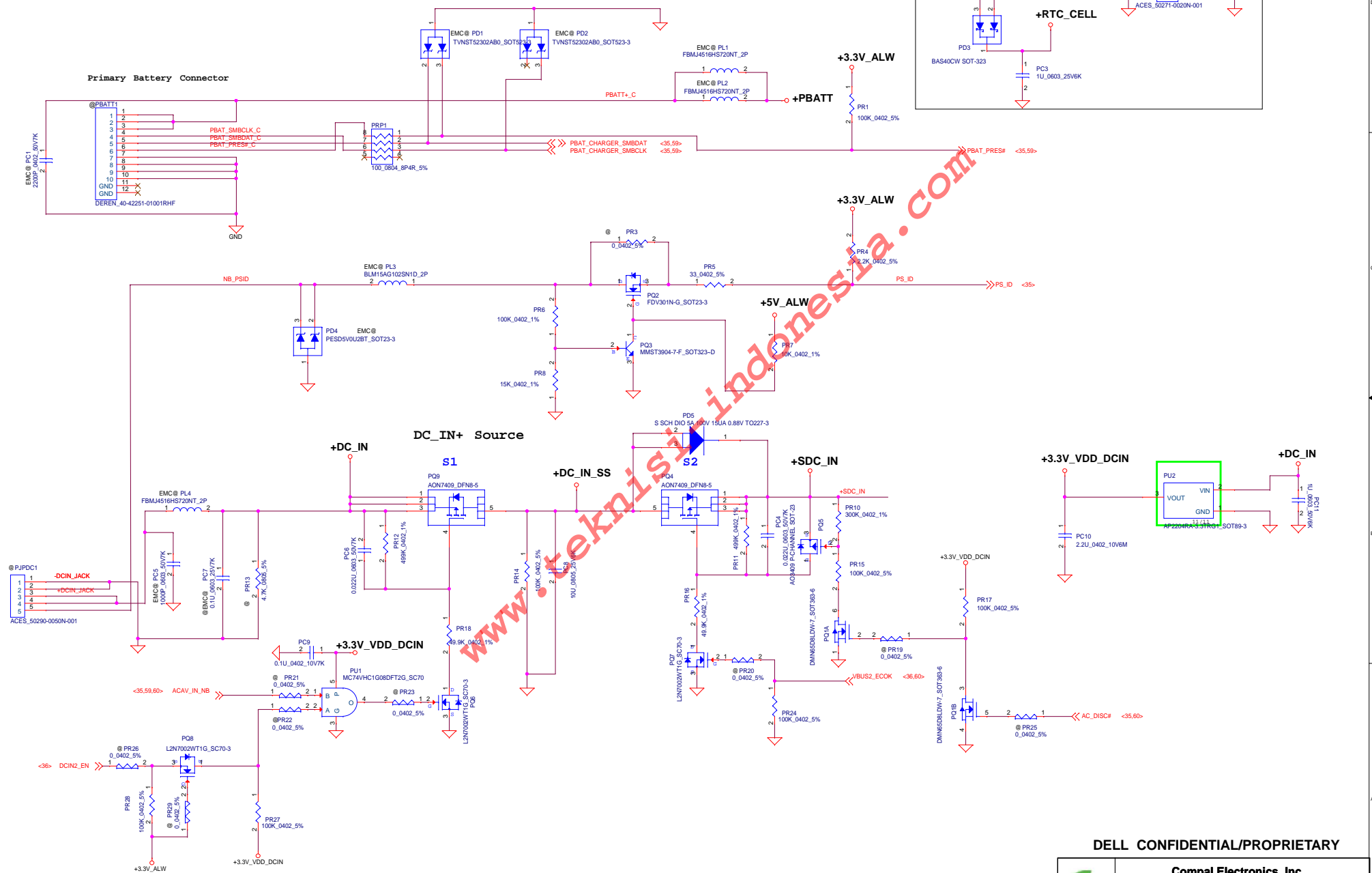
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Stack-up

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+DCIN	
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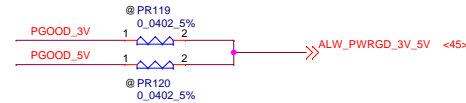
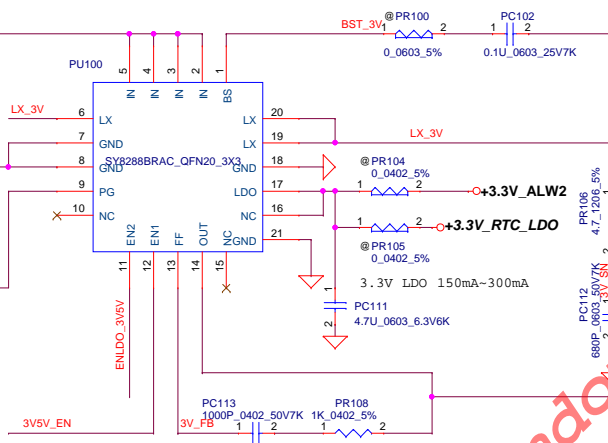
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+PWR_SRC

PJP100
PAD-OPEN 1x2m-D

+3.3V_ALW

PGOOD_3V



ENLDO_3V5V
PR102 499K_0402_1%
+PWR_SRC

+3.3V_ALWP

3VALWP
TDC 6.8 A
Peak Current 9.7A
OCP Current 14.5 A fix by I C

Vout is 3.234V~3.366V

+3.3V_ALWP
PJP102
JUMP_43X118
+3.3V_ALW

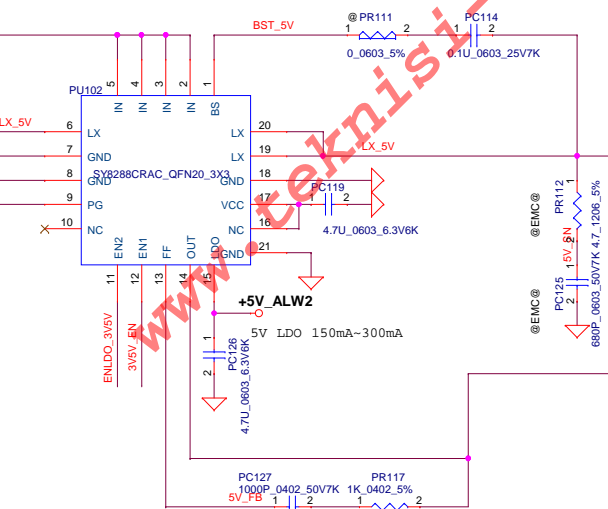
+5V_ALWP
PJP103
JUMP_43X118
+5V_ALW

+PWR_SRC

PJP101
PAD-OPEN 1x2m-D

+3.3V_ALW

PGOOD_5V



ENLDO_3V5V
3V5V_EN
+5V_ALW2
5V LDO 150mA~300mA

5VALWP
TDC 6.5A
Peak Current 9.3 A
OCP Current 14.5A fix by I C

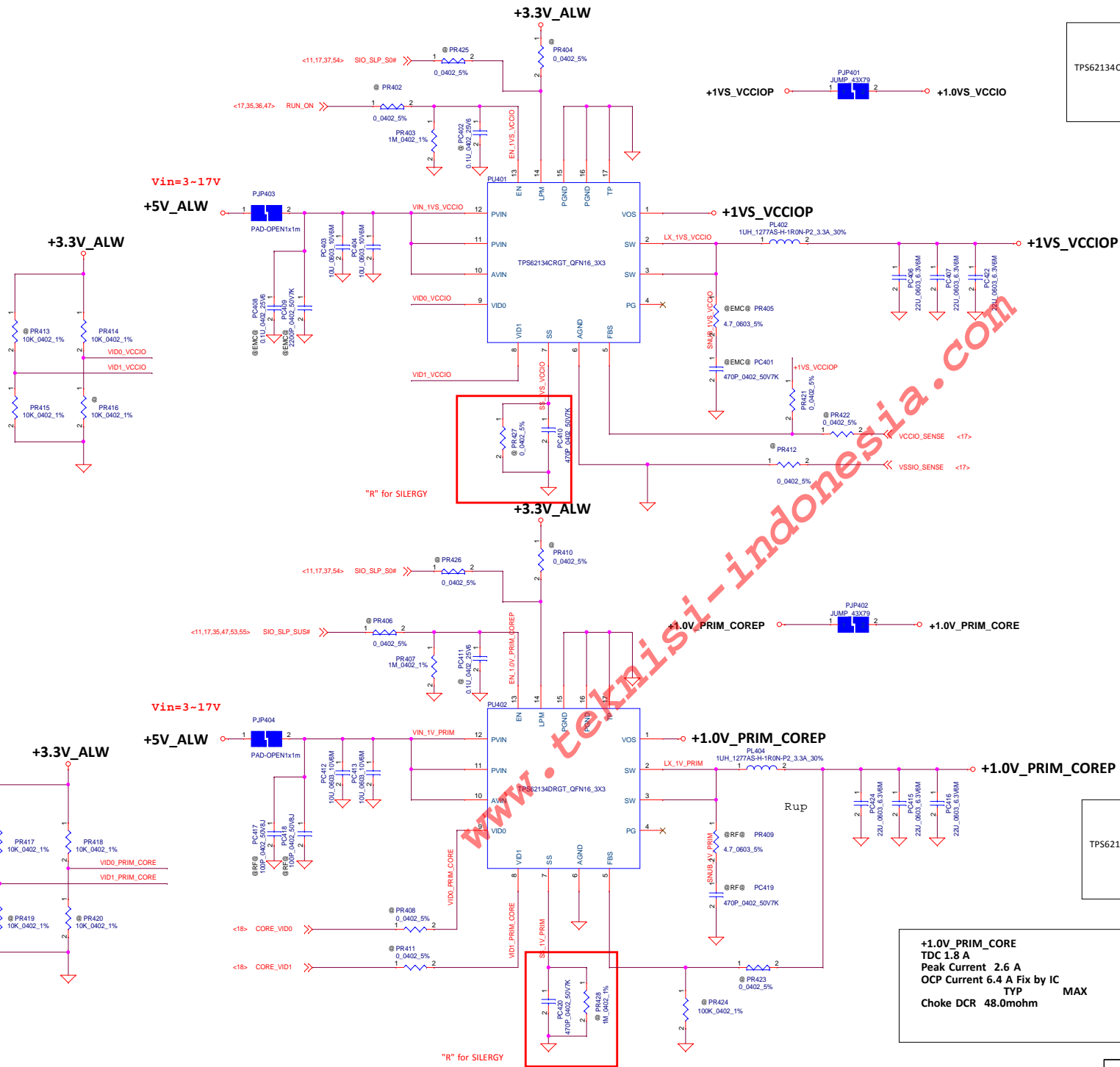
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Title		+5V_ALW/3.3V_ALW	
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	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
TPS62134C	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

+1.0VS_VCCIO
TDC 2.2 A
Peak Current 3.1 A
OCF Current 6.4 A Fix by IC
TYP
Choke DCR 48.0mohm
MAX

	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
TPS62134D	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

+1.0V_PRIM_CORE
TDC 1.8 A
Peak Current 2.6 A
OCF Current 6.4 A Fix by IC
TYP
Choke DCR 48.0mohm
MAX

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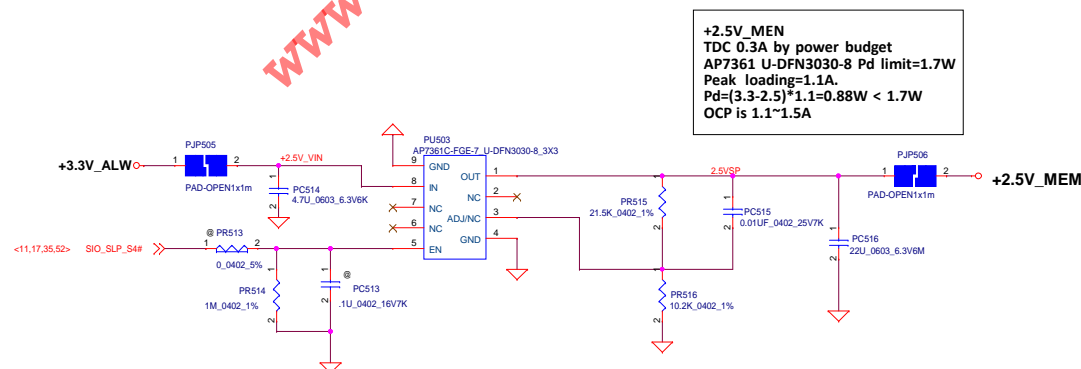
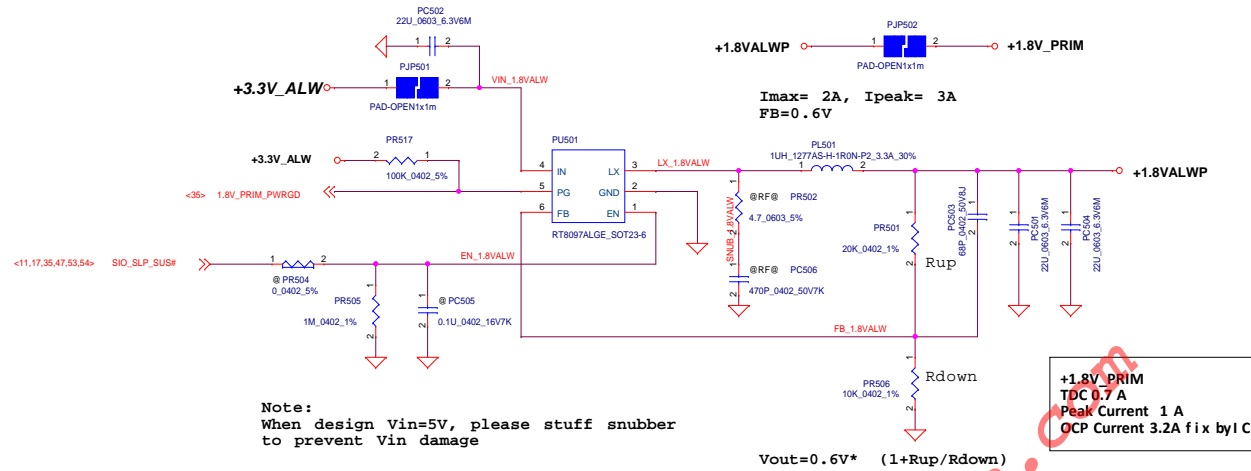
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Rev 0.5



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		Compal Electronics, Inc.	
		+1.8VALWP/+1.5VSP	
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Local sense put on HW site

+1.0V_VCCST

VCC_SA
TDC 4A
Peak Current 4.5A
OCP current 5.4A
Choke DCR 13 m ohm

VCCSA_B+
CPU_B+
PAD-OPEN1x1m

VCCSA_B+

+VCC_SA

+5V_ALW

+5V_ALW

<15> VCCSENSE

<15> VSSSENSE

Local sense put on HW site

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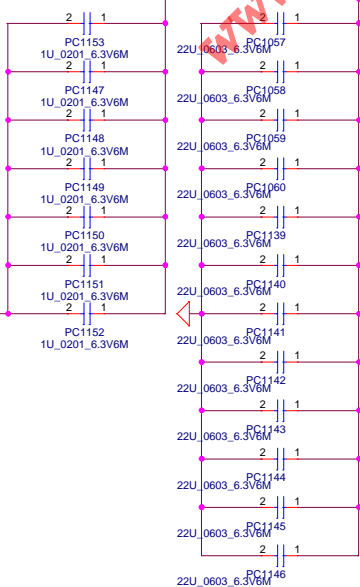
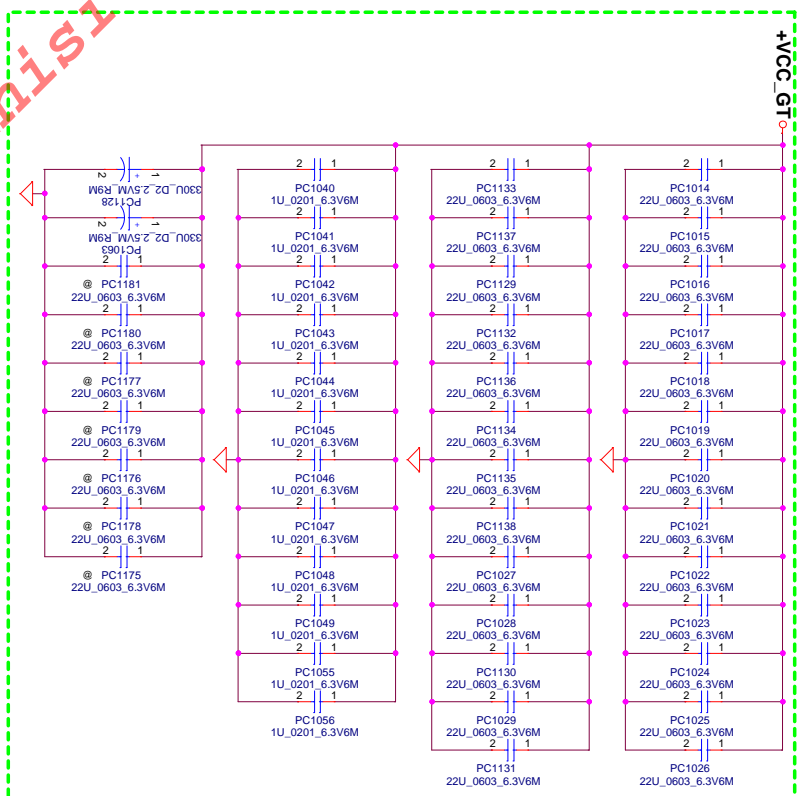


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PWR_VCORE_ISL95857

Size Document Number LA-E071P Rev 0.5
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VCC_GT_Place on CPU (U22)
22U_0603 * 26 pcs +1U_0201*12 pcs
+330u_D2*2 pcs
```

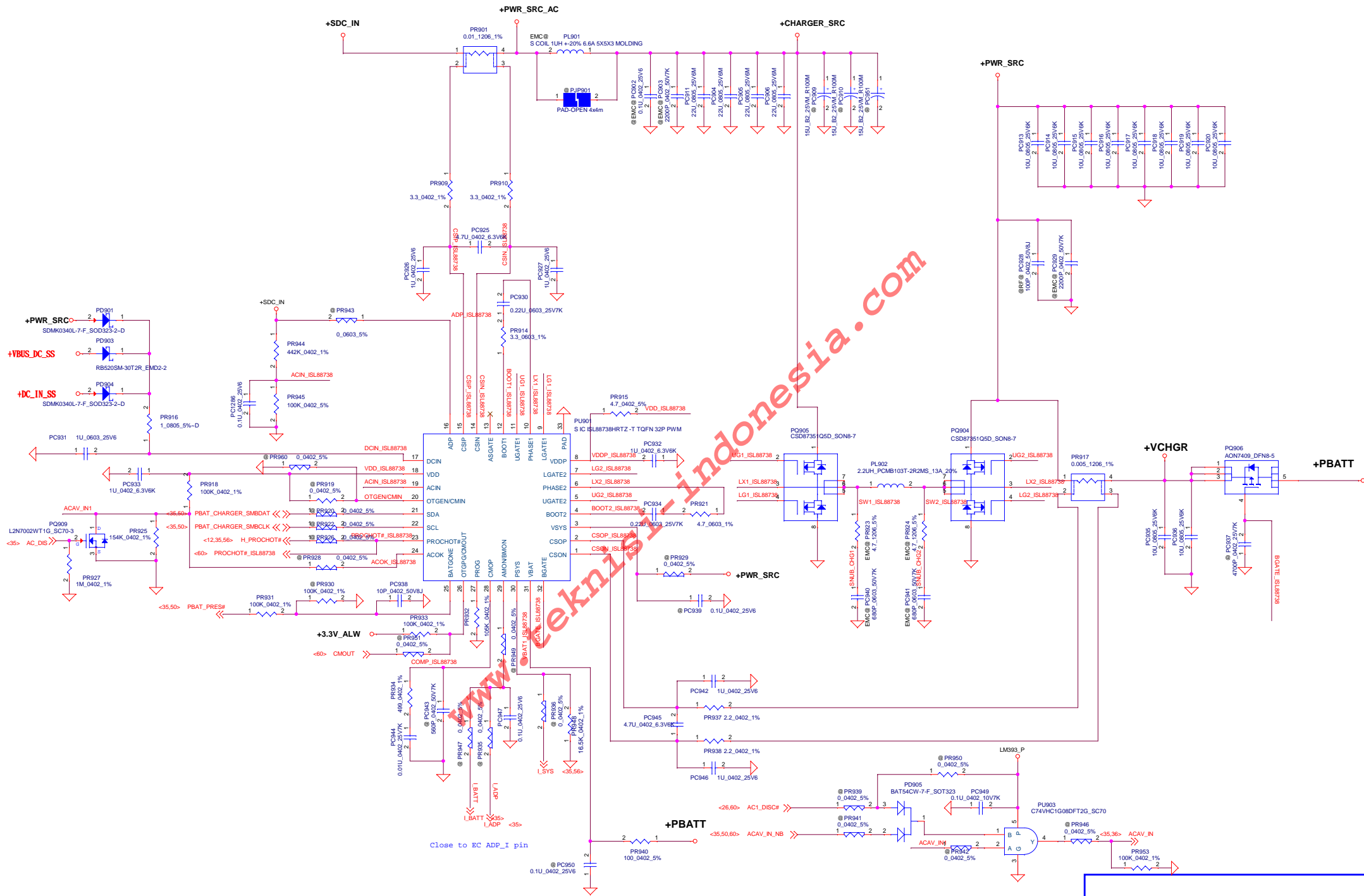


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PROCESSOR DECOUPLING

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	HW	2016/05/24	COMPAL	For Schematic align	Remove RA2	0.2(X01)
2	35	HW	2016/05/24	COMPAL	Symbol pin name change	UE1.C1 pin name change to GPIO024/nRESETI	0.2(X01)
3	9	HW	2016/05/24	COMPAL	Symbol pin name change	UT5.A6/A7/A8/B7 pin name change to GND, UT5.D6 pin name change to HRESET	0.2(X01)
4	25	HW	2016/05/24	COMPAL	Symbol pin name change	UT9.20 pin name change to SNK_CAD/DCI_DAT, UT9.32 pin name change to HPDIN/DCI_CLK	0.2(X01)
5	6	HW	2016/05/24	COMPAL	DP HPD base on INTEL PDG	Delete RC312/RC242	0.2(X01)
6	25	HW	2016/05/24	COMPAL	Disable AUX snoop feature	Pop RT308	0.2(X01)
7	33,40	HW	2016/05/24	COMPAL	Remove HDD LED MUX feature	Depop RN100/RN101	0.2(X01)
8	35	HW	2016/05/24	COMPAL	PORT80_DET#	Reserve RE513,100k (SD028100380) to GND	0.2(X01)
9	6	HW	2016/05/24	COMPAL	Follow Intel PDG AUX topology	Delete RC179/RC180/RC181/RC182 Add test point T281/T282 for CPU_DP1_AUXN and CPU_DP1_AUXP	0.2(X01)
10	17	HW	2016/05/24	COMPAL	S0ix(modern standby) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
11	46	HW	2016/05/24	COMPAL	For DFX request	H1/H2/H3/H4/H7/H8/H34 footprint remove "-G"	0.2(X01)
12	25	HW	2016/05/27	COMPAL	For Schematic align	SW2_DP1_HPD Add RT380 place near TUSB546	0.2(X01)
13	30	HW	2016/06/01	INTEL	Intel reviwie result	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(@_0201 to 10uF_0603 CZ32/CZ31/CZ29 place near JNGFF1.2/JNGFF1.4 CZ27/CZ30/CZ28 place near JNGFF1.72/JNGFF1.74	0.2(X01)
14	37,38	HW	2016/06/07	DELL	change to Nuvoton TPM form ATMEL TPM	Delete ATMEL TPM circuit, Add Nuvoton TPM circuit	0.2(X01)
15	12	HW	2016/06/07	INTEL	Intel MOW request	Add CC331 2.2PF (SE07122AC80) for HDA_RST# Add CC332 2.2PF (SE07122AC80) for HDA_SDIN0 Add CC333 2.2PF (SE07122AC80) for HDA_SDOUT	0.2(X01)
16	33	HW	2016/06/07	INTEL	Intel reviwie result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
17	33	HW	2016/06/07	COMPAL	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
18	35	HW	2016/06/07	COMPAL	For MEC5105K-D1-TN sample	1.UE1 change to SA00009GL00(S IC MEC5105K-D1-TN WFBGA 169P EC) 2.Depop RE361,Pop RE360,RE362	0.2(X01)
19	41	HW	2016/06/17	COMPAL	BITS284924-HDD is still working after press power button into S5 during POST.	Depop RN5	0.2(X01)
20	38,45	HW	2016/06/20	COMPAL	ME request	1.JKBTP1 change from HRS_TF49-20S-0P5SH_20P-T to CIVILU_CF5020FD0RK-05-NH_20P-T 2.JUSH1 change from HRS_TF49-26S-0P5SH_26P-T to CIVILU_CF5026FD0RK-05-NH_26P-T DELL CONFIDENTIAL/PROPRIETARY	0.2(X01)

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21	34	HW	2016/06/20	COMPAL	Base on Audio EA result	RA7,RA8 change from 24.9 to 16.2 ohm(SD00001U900)	0.2(X01)
22	30	HW	2016/06/22	COMPAL	EMI request	CL22 change from 1500pF to 10pF (SE167100J80 S CER CAP 10P 3KV J NPO 1808 AC250V X2Y3)	0.2(X01)
23	30	HW	2016/06/22	COMPAL	ESD request	Reserve DL1 SCA00000T00 (S ZEN ROW PESD5V0U2BT 3P C/C SOT23 ESD)	0.2(X01)
24	29	HW	2016/06/22	COMPAL	EMI request	Change LV1 from SM01000BV00 to SM01000NY00	0.2(X01)
25	29	HW	2016/06/22	COMPAL	ME request	JIR1 change from SP010023D00 to SP010013W20	0.2(X01)
26	35	HW	2016/06/22	DELL	The possibility of GPIO map update,RTCRST_ON change from GPIO141 to GPIO122	Add RE514(@),RE515 for RTCRST_ON	0.2(X01)
27	36	HW	2016/06/22	COMPAL	For pre-config TPM	POP RZ363, De-POP RZ112,RZ113,RZ111,QZ9	0.2(X01)
28	29	HW	2016/06/22	COMPAL	RF request	CC27 pop 47pF	0.2(X01)
29	38	HW	2016/06/29	COMPAL	X8 have no difference JUSH1 pin define concern	Depop DZ7,Pop RZ87	0.2(X01)
30	38	HW	2016/06/29	COMPAL	Let USH_PWR_STATE# keep low at S5	RZ10 change from 1M to 100k ohm	0.2(X01)
31	36	HW	2016/06/29	COMPAL	Foe X01 Board ID	RE79 change from 240k to 130k ohm	0.2(X01)
32	24	HW	2016/07/04	COMPAL	For VGA test result	Pop RV121/RV122/CV132/CV133	0.2(X01)
33	41	HW	2016/06/29	COMPAL	BITS283552 - [BR_CSLP] FFS AP no function when execute FF generator or shake SU	FFS VDD_IO change to +3.3V_RUN	0.2(X01)
34	35, 36	HW	2016/08/04	COMPAL	Vendor schematic review	1. Add net WRST# to UE2.4 and CE500 1uf (SE000000K80) 2. Add RE523 0 ohm for UE2 power pin soft start 3. Change RE14,RE15,RE18 from 100k ohm to 10k ohm 4. Change RPE12.1 to RE524 (10Kohm) for EXPANDER_GPU_SMDAT 5. Change RPE12.2 to RE525 (10Kohm) for EXPANDER_GPU_SMCLK 6. Reserve CE504~CE505 for EXPANDER_GPU_SMDAT/CLK to GND.	0.3(X02)
35	14	HW	2016/08/04	COMPAL	Intel suggestion	RC137 change from 1K to 3K	0.3(X02)
36	27	HW	2016/08/04	COMPAL	For UT7 2nd source issue	Add RT393 PD 100K ohm to +5V_PD_VDD for discharging instantly	0.3(X02)
37	45	HW	2016/08/04	COMPAL	Touchpad I2C EA	Chagne RZ20, RZ21 from 4.7k ohm to 2.2k ohm Change CZ80, CZ81 from 330pf to 10pf	0.3(X02)
38	26	HW	2016/08/04	COMPAL	For PD sample	Change UT5 from SA00009W200 to SA00009W210	0.3(X02)
39	33, 38	HW	2016/08/09	COMPAL	DFB request	SMT concern DZ1, DZ2, DZ5, DZ6 PCB pad is too small, suggest use the symbol "RB520SM-30T2R_EMD2-2" follow PD903	0.3(X02)
40	34, 36	HW	2016/08/10	COMPAL	Footprint align	DA8, DE1 follow symbol "RB520SM-30T2R_EMD2-2"	0.3(X02)
41	46	HW	2016/08/11	COMPAL	ME request	H9 footprint change from "H_2P8-G" to "H_2P8"	0.3(X02)
42	36	HW	2016/08/11	COMPAL	schematic align	add power rail +3.3V_ALW_UE2 for UE2	0.3(X02)

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43	31	HW	2016/08/30	COMPAL	[ME] SD card issue	1. change JSD1 form "T-SOL_156-2000302608" to "T-SOL_158-1000902614" 2. QR1.3 connect GND	0.4(X02)
44	35	HW	2016/08/30	COMPAL	battery life	USH_DET# reserve RE526 (10K) PU to +3.3V_Run, follow X7	0.4(X02)
45	37	HW	2016/09/08	COMPAL	TPM change to NPCT650VB2YX	Change UZ12 from to SA00008EL70 to SA00008EL80	0.5(X03)
46	35, 36	HW	2016/09/08	COMPAL	Expander I/O change from ITE8010 to MCP23008	Change UE2 from SA00009VL00 to SA0000ADQ00, remove RE523 Change RE524, RE525 from 10Kohm to 2.2Kohm	0.5(X03)
47	35	HW	2016/09/08	COMPAL	Board ID	Change RE79 to 33kohm (SD028330280)	0.5(X03)
48	35	HW	2016/09/08	COMPAL	schematic align	Reserve RE526(10K) PU for USH_DET# to +3.3V_ALW	0.5(X03)
49	35	HW	2016/09/08	COMPAL	EC request for power consumption	Add RE505 PU to +3.3V_ALW for LOM_CABLE_DETECT# (Reserve) Add RE532 PU to +3.3V_ALW for BCM5882_ALERT#	0.5(X03)
50	38	HW	2016/09/08	COMPAL	USH/B de-pop, pop on MB side	POP RZ8,RZ9 for USH SMBus	0.5(X03)
51	36	HW	2016/09/20	COMPAL	DELL request	Add RE536/RE537 for resistors for PCH_DPWROK circuit	0.5(X03)
52	35	HW	2016/09/20	COMPAL	WDT schematic option 2	use Option2: pop RE361 / depop RE362	0.5(X03)
53	34	HW	2016/09/20	COMPAL	EMI request	1. L6-L9 change to 80ohm bead (BLM15PD800SN1D, SM01000N000) for BR14/15 2. depop CA2, CA3 3. RA55,RA56 need to netin for changing location(LA15, LA16) with 33ohm bead (BLM15PX330SN1D,SM01000NA00)	0.5(X03)
54	36	HW	2016/10/09	COMPAL	BITS294007 - Sometimes need to press power button twice to power on system	CE12 change to 2.2u (SE000008880) RE33 change to 1K (SD028100180)	0.5(X03)
55	24	HW	2016/10/09	COMPAL	U-line VGA EA PASS	depop RV121/RV122	0.5(X03)
56	26	HW	2016/10/09	COMPAL	TI CC pin for ESD request	CT85,CT86 change to 470p.(SE074471k80)	0.5(X03)
57	26	HW	2016/10/31	COMPAL	TI CC pin for EA	CT85,CT86 change to 820p.(SE000003W80)	1.0(A00)
58	26	HW	2016/10/31	COMPAL	EC watchdog reserve	add QE13,RE530,CE503	1.0(A00)
59	26	HW	2016/10/31	COMPAL	UE1.H8 to prevent EOS issue on MEC5105	Add RE539(100ohm) to CV2_ON	1.0(A00)
60	36	HW	2016/10/31	COMPAL	BOARD ID	Change RE79 to 4.3k ohm(SD028430180)	1.0(A00)
61	36	HW	2016/10/31	COMPAL	Change R1 to R3 for MP part	Change UL1 CP/N to SA000081G1L Change UE1 CP/N to SA00009GL30	1.0(A00)
62	36	HW	2016/10/31	COMPAL	For DFB request.	Close solder mask CMOS1 (-NPM) and other co-lay part	1.0(A00)
63	36	HW	2016/10/31	COMPAL	Service Mode Switch remove	Depop SW1 and RC222 and RC221 change to short pad	1.0(A00)
64	36	HW	2016/10/31	COMPAL	RE374 change BS to LPC@	RE374 change BS to LPC@	1.0(A00)
65	36	HW	2016/10/31	COMPAL	For MEC5105 rev. C	Pop RE362,RE536; Depop RE361,QE13,CE503,RE530,UE7,CE5,CE6,RE348,RE537	1.0(A00)

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